DAMPING POWER SYSTEM OSCILLATIONS USING AN SSSC-BASED HYBRID SERIES CAPACITIVE COMPENSATION SCHEME

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By

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ABSTRACT

Interconnection of electric power systems is becoming increasingly widespread as part of the power exchange between countries as well as regions within countries in many parts of the world. There are numerous examples of interconnection of remotely separated regions within one country. Such are found in the Nordic countries, Argentina, and Brazil. In cases of long distance AC transmission, as in interconnected power systems, care has to be taken for safeguarding of synchronism as well as stable system voltages, particularly in conjunction with system faults. With series compensation, bulk AC power transmission over very long distances (over 1000 km) is a reality today. These long distance power transfers cause, however, the system low-frequency oscillations to become more lightly damped. As a result, many power network operators are taking steps to add supplementary damping devices in their systems to improve the system security by damping these undesirable oscillations. With the advent of voltage sourced converter-based series compensation, AC power system interconnections can be brought to their fullest benefit by optimizing their power transmission capability, safeguarding system stability under various operating conditions and optimizing the load sharing between parallel circuits at all times.

This thesis reports the results of digital time-domain simulation studies that are carried out to investigate the effectiveness of a phase imbalanced hybrid single-phase-Static Synchronous Series Compensator (SSSC) compensation scheme in damping power system oscillations in multi-machine power systems. This scheme, which is feasible, technically sound, and has an industrial application potential, is economically attractive when compared with the full three-phase-SSSC.

Time-domain simulations are conducted on a benchmark model using the ElectroMagnetic Transients Program (EMTP-RV). The results of the investigations have demonstrated that the hybrid single-phase-SSSC compensation scheme is very effective in damping power system oscillations at different loading profiles.

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LIST OF SYMBOLS

AC, ac	alternating current
C	capacitor
C_{dc}	dc capacitor of SSSC
CIGRE	Conseil International des Grands Réseaux Électriques (International Council on Large Electric Systems)
d	direct axis
DC, dc	direct current
E_{fd}	exciter output voltage
EMTP-RV	ElectroMagnetic Transient Program – Restructured Version
E_R	output voltage of the voltage regulator amplifier
E_{ref}	reference voltage of the excitation system
E_{SB}	feedback stabilizing signal of the excitation system
Fixed C	Transmission lines are compensated with series capacitor
e_d, e_q	d- and q- axis stator voltages
e_{fd}	field voltage
f_s	carrier signal frequency or switching frequency
FACTS	flexible AC transmission system
$G_p(s)$	transfer function of a proportional type SSSC supplemental controller
$G_{L\text{-}L}(s)$	transfer function of a lead-lag type SSSC supplemental controller
H	inertia constant of synchronous generator
HV	high voltage
Hz	hertz
Hybrid	Transmission lines are compensated with the hybrid single-phase-SSSC compensation scheme
i_c	IGBT collector current
i_d	diode current
i_d, i_q	d- and q- axis stator currents
$I_{dc\text{-}ext}$	external dc source current
IEEE	Institute of Electrical and Electronics Engineers

i_{fd}	field winding current
i_{1d},	d-axis damper winding current
i_{1q}, i_{2q}	q-axis damper winding currents
IGBT	insulated gate bipolar transistor
i_o	output current of a single-phase dc-ac converter
i_{line}	transmission line current
I_s	diode leakage current
k	degree of compensation
K_A	gain of the voltage regulator amplifier
K_E	exciter gain
K_F	feedback stabilizing loop gain of the excitation system
K_G	supplemental controller gain
K_P	proportional controller gain
K_i	integral controller gain
kV	kilo volt
L_{ad}	d-axis magnetizing inductance
L_{aq}	q-axis magnetizing inductance
LC	inductance-capacitance
L_d, L_q	d- and q-axis synchronous inductances
LF	loop filter
L_{ffd}	self-inductance of the field winding
L_{11d}	self-inductance of the d-axis damper winding
L_{11q}, L_{22q}	self-inductances of the q-axis damper winding
LP	low-pass
LV	low voltage
m_a	amplitude modulation ratio or modulation index
m_f	frequency modulation ratio
MVA	mega volt-ampere
MW	mega watt
MVAr	mega volt-ampere reactive
P	real (active) power
PD	phase detector
PI	proportional-integral

PLL	phase-locked loop
P_{L1} *and PL1*	real power flow in transmission line L_1
P_{L2} *and PL2*	real power flow in transmission line L_2
P_m	mechanical power
POD	power oscillations damping
p.u.	per unit
PWM	pulse-width modulation
Q	reactive power
q	quadrature axis
R_a	armature resistance
R_{fd}	field winding resistance
R_L	resistance of the series capacitor compensated transmission line
R_{1d}	d-axis damper winding resistance
R_{1q}, R_{2q}	q-axis damper winding resistances
RMS	root-mean-square
s	Laplace transformation operator
S	apparent power
SPWM	sinusoidal pulse-width modulation
SPVSC	single-phase voltage-sourced converter
SSR	subsynchronous resonance
SSSC	static synchronous series compensator
SVS	synchronous voltage source
^{T}	superscript to denote matrix transpose
t	time
T_A, T_E, T_F	time constants in the excitation system
T_{ELEC}	air-gap torque
T_m	supplemental controller low-pass filter time constant
T_{MECH}	mechanical torque
T_1, T_2, T_3, T_4	lead-lag network time constants
T_w	washout filter time constant
VAR or VAr	volt-ampere reactive
V_b	infinite bus voltage

V_{bd}, V_{bq}	d- and q- axis voltages of infinite bus
V_{BR}	diode reverse breaking voltage
V_C	voltage across the series capacitor of the compensated transmission line
V_{Cd}, V_{Cq}	voltages across the series capacitor in the d-q reference frame
$\hat{V}_{carrier}$	carrier signal peak magnitude
v_{CE}	IGBT collector-emitter voltage
$\hat{V}_{control}$	control signal peak magnitude
VCO	voltage-controlled oscillator
v_{GE}	IGBT gate-emitter voltage
v_d	diode voltage
V_{dc}	dc-side voltage of SSSC or converter
$V_{dc\text{-}ext}$	external dc source voltage
v_{inj}	injected voltage
V_L	voltage across the inductance of the series capacitor compensated transmission line
V_{Ld}, V_{Lq}	voltages across the inductance in the d-q reference frame
v_o	output voltage of a single-phase dc-ac converter
V_p	in-phase component of the injected voltage
V_q	quadrature component of the injected voltage
V_R	voltage across the resistance of the series capacitor compensated transmission line
V_{Rd}, V_{Rq}	voltages across the resistance in the d-q reference frame
V_R	receiving bus voltage
V_S	sending bus voltage
VSC	voltage-sourced converter
V_{SSSC}	injected voltage by SSSC
V_t	generator terminal voltage
V_{td}, V_{tq}	d- and q- axis generator terminal voltages
X_C	series capacitor reactance
X_L	inductive reactance of the series capacitor compensated transmission line
X_{line}	series inductive reactance of the transmission line

X_{-max}, X_{-min}	maximum and minimum SSSC reactances respectively
X_{order}	dynamic reactance of SSSC
X_{SSSCo}	initial net reactance of SSSC
Y	admittance
Z	impedance
Ψ_d, Ψ_q	d- and q- axis stator flux linkages
Ψ_{fd}	field winding flux linkage
Ψ_{1d}	d-axis damper winding flux linkage
Ψ_{1q}, Ψ_{2q}	q-axis damper winding flux linkages
δ	generator power (load) angle
δ_{21} *and d21*	generator 2 load angle measured with respect to generator 1 load angle
δ_{31} *and d31*	generator 3 load angle measured with respect to generator 1 load angle
δ_R	receiving bus load angle
δ_S	sending bus load angle
ζ	control parameter
Θ	angle of the control signal
Θ_{sys}	angle of the transmission system
ω	angular velocity
ω_0 (f_0)	synchronous frequency (377 rad/sec)
ω_{21}	generator 2 speed measured with respect to generator 1 speed
ω_{31}	generator 3 speed measured with respect to generator 1 speed
0	suffix to denote the initial operating condition
-1	superscript to denote matrix inversion

Chapter 1

INTRODUCTION

1.1 General

Growth of electric power transmission facilities is restricted despite the fact that bulk power transfers and use of transmission systems by third parties are increasing. Transmission bottlenecks, non-uniform utilization of facilities and unwanted parallel-path or loop flows are not uncommon. Transmission system expansion is needed, but not easily accomplished. Factors that contribute to this situation include a variety of environmental, land-use and regulatory requirements. As a result, the utility industry is facing the challenge of the efficient utilization of the existing AC transmission lines. Thus, the transmission systems are being pushed to operate closer to their stability and thermal limits. Although electricity is a highly engineered product, it is increasingly being considered and handled as a commodity. Thus, the focus on the quality of power delivered is also greater than ever.

Series capacitive compensation of power transmission lines is an important and the most economical way to improve power transfer capability, especially when large amounts of power must be transmitted through long transmission lines. However, one of the impeding factors for the increased utilization of series capacitive compensation is the potential risk of Subsynchronous Resonance (SSR), where electrical energy is exchanged with turbine-generator shaft systems in a growing manner which can result in shaft damage [1]. Figure 1.1 shows a typical time response of a turbine-generator shaft torsional torque during and after clearing a fault on a series capacitive compensated transmission line in the presence of the SSR phenomenon. It is worth noting here that this shaft is designed to withstand a maximum torsional torque of 2 per unit. Another limitation of series capacitive compensation is its inability to provide adequate damping to power system oscillations after clearing system faults. Figure 1.2 shows a typical time response of a generator load angle, measured with respect to a reference generator load angle, during and after clearing a three-phase fault on a series capacitive compensated transmission line. As it can be seen from this figure, the oscillations are not

completely damped after the first few seconds from fault clearing which results in degrading the power quality of the system.

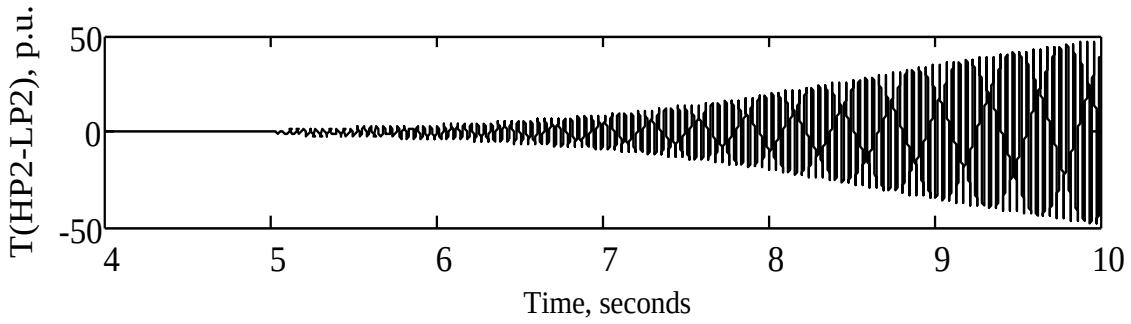


Figure 1.1: Transient time response of a turbine-generator shaft torsional torque during and after clearing a system fault on a series capacitive compensated transmission line.

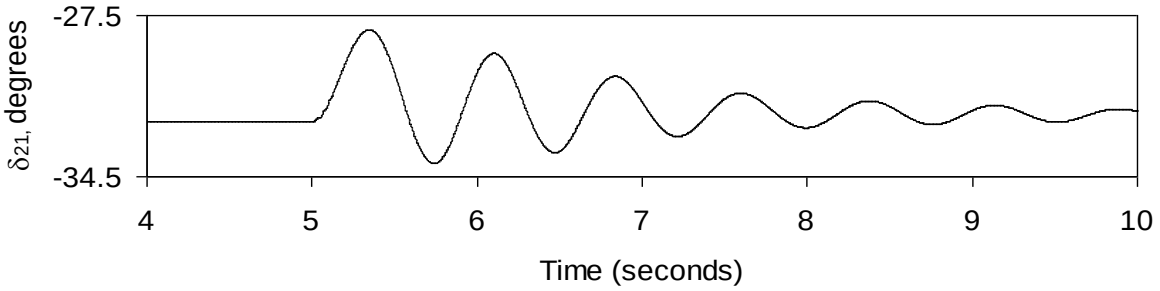


Figure 1.2: Transient time response of a generator load angle, measured with respect to a reference generator load angle, during and after clearing a system fault on a series capacitive compensated transmission line.

1.2 Transmission Line Series Compensation

The main purpose of series compensation in a power system is virtual reduction of line reactance in order to enhance power system stability and increase the loadability of transmission corridors [2]. The principle is based on the compensation of the distributed line reactance by the insertion of a series capacitor. The reactive power generated by the capacitor is continuously proportional to the square of the line current. This means that the series capacitor has a self-regulating effect. When the system loading increases, the reactive power generated by the series capacitor increases as well. The response of the series capacitor is automatic, instantaneous and continuous as long as the capacitor current remains within the specified operating limits. The following are some of the major benefits of incorporating series capacitors in transmission systems:

1.2.1 Steady-state voltage regulation

A series capacitor is capable of compensating the voltage drop of the series inductance of a transmission line. Referring to Figure 1.3, during light loading (Load L), the voltage drop on the series capacitor is low. When the load increases (Load H) and the voltage drop on the line becomes larger, the contribution of the series capacitor increases and, therefore, the system voltage at the receiving line end will be regulated as desired.

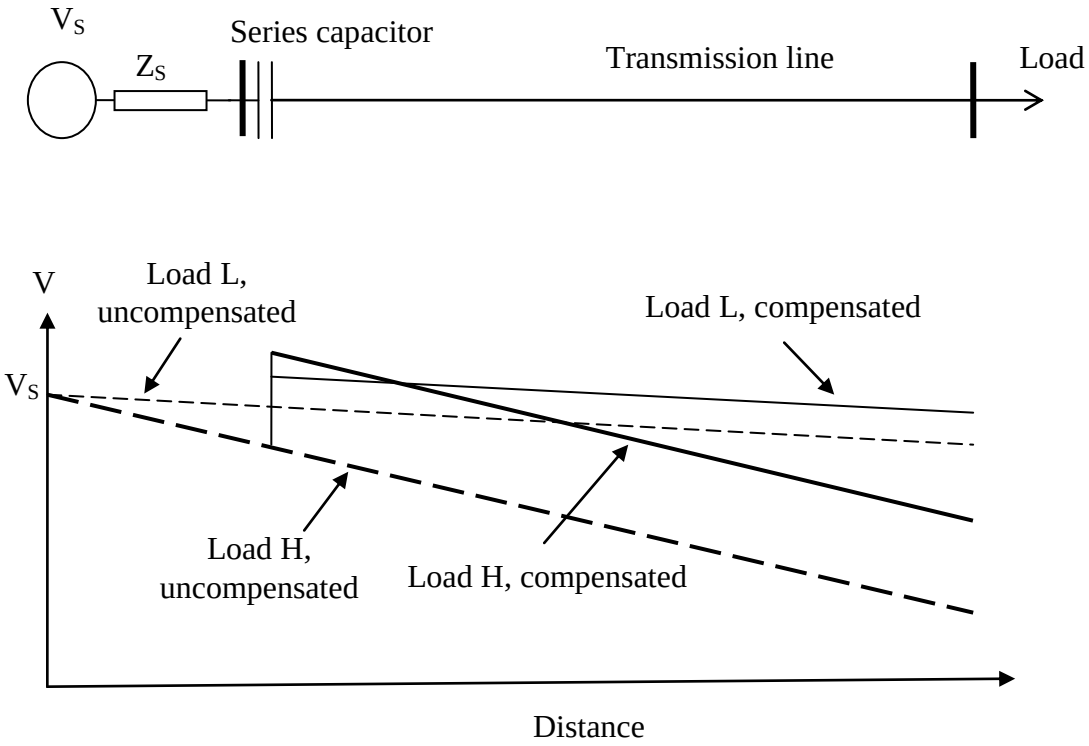


Figure 1.3: A simple radial power system and voltage drop compensation with a series capacitor.

1.2.2 Increase in the power transfer capability by raising the first swing stability limit

A substantial increase in the stability margin is achieved by installing a series capacitor. The series compensation will improve the situation in two ways: it will decrease the initial generator load angle corresponding to a specific power transfer and it will also shift the power-load angle (P-δ) characteristic upwards. This will result in increasing the transient stability margin.

1.2.3 Increase in power transfer

The increase in the power transfer capability as a function of the degree of compensation for a transmission line can be illustrated using the circuit and the vector diagram shown in Figure 1.4. The power transfer on the transmission line is given by:

$$P = \frac{|V_S||V_R|}{X_{line} - X_C}\sin\delta = \frac{|V_S||V_R|}{X_{line}(1-k)}\sin\delta \tag{1.1}$$

Where *k* is the degree of compensation defined as

$$k = \frac{X_C}{X_{line}} \tag{1.2}$$

The effect on the power transfer when a constant load angle difference is assumed is shown in Figure 1.5. Practical compensation degree ranges from 20 to 70 percent. Transmission capability increases of more than two times can be obtained in practice.

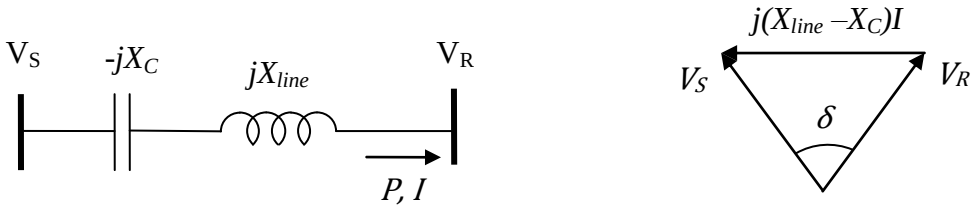


Figure 1.4: Transmission line with a series capacitor.

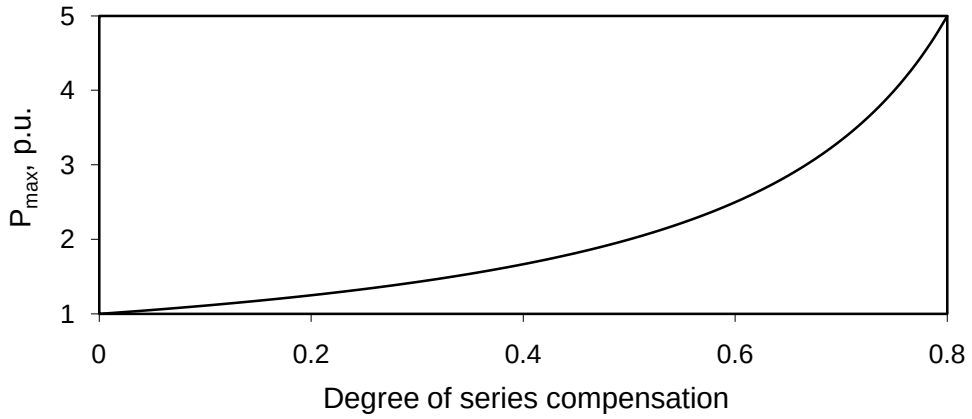


Figure 1.5: Maximum power transmitted over a transmission line as a function of the degree of series compensation ($|V_S| = |V_R| = 1\ p.u.,\ X_{line} = 1\ p.u.$).

1.2.4 Active load sharing between parallel circuits

When two transmission lines are connected in parallel, the natural power sharing between them is dictated by their respective impedances. If the two lines are of different configurations (and consequently of different thermal ratings), their impedances could still be very close. Therefore, the power transmitted in each line will be similar. The voltage drop in both circuits is identical, and therefore, the relationship between the line currents I_{L1} and I_{L2} can be expressed as:

$$I_{L1}Z_{L1} = I_{L2}Z_{L2} \tag{1.2}$$

If overloading the lower thermal rating line, (L_2, Figure 1.6) is to be avoided (i.e., $I_{L2} \leq I_{L2max}$), then the full power capacity of the other line, L_1, will never be reached (i.e., $I_{L1} < I_{L1max}$). For example, consider the case when L_1 is a four conductor bundle (quad) circuit configuration, whereas L_2 has a two conductor bundle (twin) circuit configuration. If the conductors of the two bundles are identical, then L_1 has twice the rating of L_2. The inductive reactances of the two lines, however, are very close. If a series capacitor is installed in the higher thermal rating line, both transmission lines can operate at their maximum capacity when the appropriate degree of compensation is provided (50% in this case) [3].

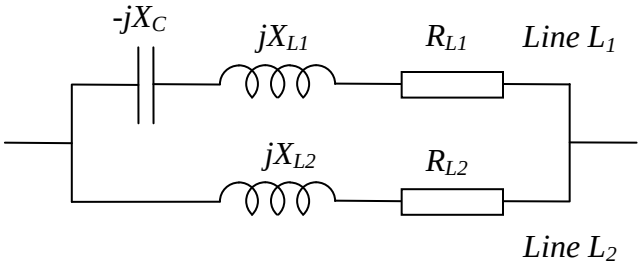


Figure 1.6: Adjusting the power sharing between two parallel lines using a series capacitor.

1.3 Series Capacitor Location

The optimum location for a single series capacitor bank, in terms of the most effective use of the series capacitive reactance, is at the middle of the transmission line [2]. The "effectiveness", which is based on the distributed parameter theory of transmission lines, is the figure of merit for the reduction of the series inductive reactance by a series capacitor. One Canadian installation that has the capacitors located at the middle of the transmission line is the

B.C. Hydro 500 kV system described in [4]. A number of utilities, especially in the U.S., have tended to utilize two series capacitor banks and locate them at the ends of the transmission lines, in order to take advantage of existing land and the availability of service personnel at the line terminals [2]. In some situations, there may be valid reasons (geographical restrictions or specific benefits) for selecting other locations. For example, B.C. Hydro has a 605 MVAr, 500 kV single capacitor bank installed at McLeese substation which is located "nearly" mid-line between Williston and Kelly Lake substations (180 km from Williston and 130 km from Kelly Lake) [5].

1.4 Power System Oscillations

Many electric utilities world-wide are experiencing increased loadings on portions of their transmission systems, which can, and sometimes do, lead to poorly damped, low-frequency oscillations (0.5 – 2 Hz). These oscillations can severely restrict system operations by requiring the curtailment of electric power transfers as an operational measure. They can also lead to widespread system disturbances if cascading outages of transmission lines occur due to oscillatory power swings, like during the blackout in Western North America on August 10, 1996 [6].

Damping is defined as the energy dissipation properties of a material or a system. Power system oscillations can be damped, when extra energy is injected into the system which is instantaneously decelerated, and/or when extra energy is consumed in the system which is instantaneously accelerated. The damping energy is obtained by the modulation of load or generation for a period of time, typically in the range of five to ten seconds. The damping energy must have the correct phase shift relative to the accelerated/decelerated system as incorrect phase angles can excite the oscillations. Figure 1.7 shows different possibilities to damp power system oscillations [7].

1.5 Flexible AC Transmission Systems

All of the above discussed advantages of series compensation can be achieved without the risks of SSR phenomenon if series Flexible AC Transmission Systems (FACTS) devices are used instead of series capacitors. These devices are also able to provide adequate and fast damping to power system to oscillations.

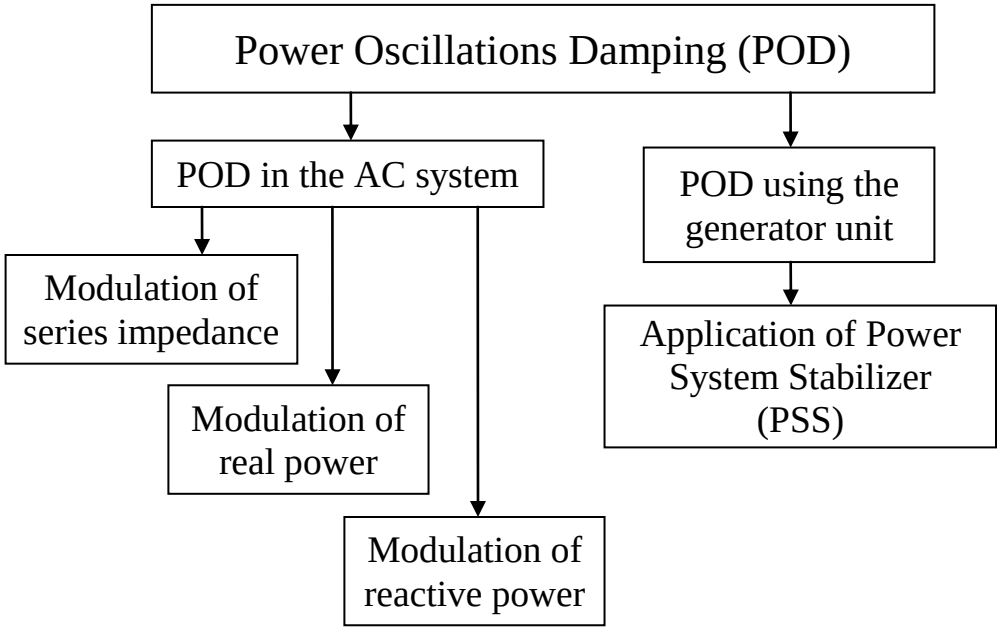


Figure 1.7: Strategies to damp power system oscillations.

FACTS Controllers are power electronic based controllers which can influence transmission system voltages, currents, impedances and/or phase angles rapidly [8], [9]. These controllers have the flexibility of controlling both real and reactive power, which could provide an excellent capability for improving power system dynamics. FACTS technology provides an unprecedented way for controlling transmission grids and increasing transmission capacity.

FACTS Controllers can be classified in two ways. They can be categorized according to their connection into the power system (series or shunt) or according to their power electronic configuration (thyristor-based or Voltage-Sourced Converter (VSC)-based types). For example, the Thyristor-Controlled Series Capacitor (TCSC) is a thyristor type series-connected controller, the Static Synchronous Series Compensator (SSSC) is a VSC type series-connected, the Static Var Compensator (SVC) is a thyristor type shunt-connected controller, the Static Series Compensator (STATCOM) is a VSC type shunt-connected controller and the Unified Power Flow Controller (UPFC) is a VSC type combined-shunt-series-connected controller. In studies conducted in this thesis, attention is focused on the SSSC Controller. The SSSC is a powerful FACTS Controller that can provide series capacitive compensation as well as it has the ability to damp power system oscillations.

1.5.1 The static synchronous series compensator

The Static Synchronous Series Compensator is a series-connected converter-type FACTS device. Although no stand-alone SSSC has been in service, the series converter of the Unified Power Flow Controller (UPFC) at the Inez Substation of the American Electric Power (AEP) system in Kentucky, USA represents an SSSC [10]. SSSC uses VSC to inject into the transmission line an almost sinusoidal voltage with independently controllable magnitude and phase angle. The SSSC uses a controller that can rapidly change the injected voltage into the transmission line. This gives the SSSC the capability to dynamically exchange reactive and/or active power with the power system. This injected voltage is almost in quadrature with the line current. The very small part of the voltage which is in phase with the line current provides the losses in the converter. The big part of the injected voltage which is in quadrature with the line current emulates an inductive or a capacitive reactance in series with the transmission line. This fast-changing emulated variable voltage dynamically influences the power flow in the transmission line. Figure 1.8 shows a typical schematic representation of an SSSC.

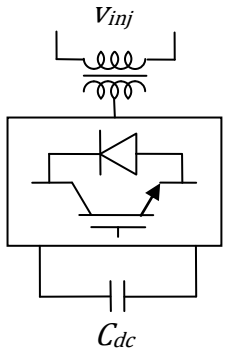


Figure 1.8: A schematic representation of an SSSC.

Because capacitors are cheaper than power electronic elements, SSSC is less competitive than fixed series compensation in terms of price. In order to reduce the overall cost, a hybrid scheme can be employed. In such a scheme, the capacitive compensation in each phase is shared between an SSSC and a fixed capacitor as shown in Figure 1.9. The reduction of the MVAr of the SSSC also implies a corresponding reduction in the conduction and switching losses in the VSC.

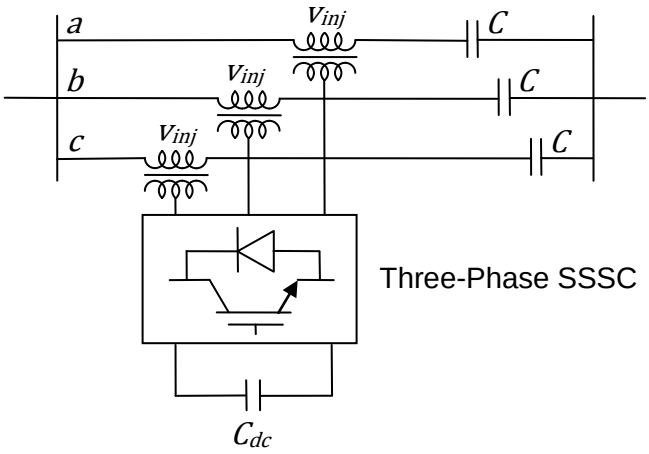


Figure 1.9: A three-line diagram of a hybrid three-phase-SSSC compensation scheme.

1.6 Research Objective and Scope of the Thesis

Analytical and simulation studies have shown that the hybrid three-phase-SSSC compensation scheme exhibits superior performance in power flow control and low-frequency and SSR oscillations damping [11] – [16]. The main objective of this research work is to investigate the possibility of damping power system oscillations resulting from large disturbances (mainly transmission line faults) in multi-machine power systems using the hybrid single-phase-SSSC compensation scheme shown in Figure 1.10. This scheme, which is feasible, technically sound, and has an industrial application potential, would definitely be economically attractive when compared with the full three-phase SSSC scheme (Figure 1.9) which has been proposed for power oscillations damping. Furthermore, reducing the number of valves will also have a positive impact on system reliability when compared to the full three-phase SSSC.

The thesis is organized in five chapters, a list of references section and two appendices. The main topics of each chapter are as follows:

Chapter 1 introduces the fundamental benefits of series compensation of transmission lines. Brief introductions to SSR, FACTS Controllers and the SSSC are also presented. The objective of the research is also presented in this chapter.

In Chapter 2, the system used for the investigations conducted in this thesis is described and the detailed dynamic models of its individual components are also presented in this chapter.

The results of the digital time-domain simulations of a case study for the system during a three-phase fault are presented at the end of this chapter.

Chapter 3 presents a comprehensive description of the single-phase-SSSC. The phase imbalanced hybrid single-phase-SSSC compensation scheme and its modeling in the ElectroMagnetic Transient Program (EMTP-RV) are also presented.

Chapter 4 demonstrates the effectiveness of the proposed hybrid single-phase-SSSC compensation scheme in damping power system oscillations through time-domain simulation studies. The performance of different supplementary controller structures and stabilizing signals are also investigated.

Chapter 5 summarizes the research described in this thesis and presents some conclusions.

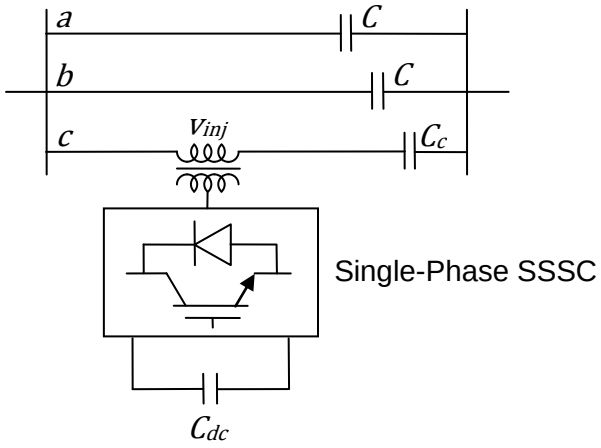


Figure 1.10: A three-line diagram of a hybrid single-phase-SSSC compensation scheme.

Chapter 2

POWER SYSTEM MODELING FOR LARGE DISTURBANCE STUDIES

2.1 General

In this chapter, the system used for the studies reported in this thesis is described and the mathematical models of its various components are presented. A digital time-domain simulation of a case study of the system during a three-phase fault is presented at the end of this chapter.

2.2 System under Study

The system used in the investigations of this thesis is shown in Figure 2.1. It consists of three large generating stations (G_1, G_2 and G_3) supplying two load centers (S_1 and S_2) through five 500 kV transmission lines. The two double-circuit transmission lines L_1 and L_2 are series compensated with fixed capacitor banks located at the middle of the lines. The compensation degree of L_1 and L_2 is 50%. The total installed capacity and peak load of the system are 4500 MVA and 3833 MVA respectively. Shunt capacitors are installed at buses 4 and 5 to maintain their voltages within 1±0.05 p.u. The system data are given in Appendix A.

2.3 Power System Modeling

The nonlinear differential equations of the system under study are derived by developing individually the mathematical models which represent the various components of the system, namely the synchronous generator, the excitation system, the transmission line and the system load. Knowing the mutual interaction among these models, the whole system differential equations can be formed.

2.3.1 Modeling of the synchronous machine

In a conventional synchronous machine, the stator circuit consisting of a three-phase winding produces a sinusoidally space distributed magnetomotive force. The rotor of the machine carries the field (excitation) winding which is excited by a dc voltage. The electrical

damping due to the eddy currents in the solid rotor and, if present, the damper winding is represented by three equivalent damper circuits; one on the direct axis (d-axis) and the other two on the quadrature axis (q-axis). The performance of the synchronous machine can be described by the equations given below in the d-q reference frame [17]. In these equations, the convention adopted for the signs of the voltages and currents are that *e* is the impressed voltage at the terminals and that the direction of positive current *i* corresponds to generation. The sign of the currents in the equivalent damper windings is taken positive when they flow in a direction similar to that of the positive field current as shown in Figure 2.2.

With time *t* expressed in seconds, the angular velocity ω expressed in rad/s (ω_0=377 *rad/sec*) and the other quantities expressed in per unit, the stator equations become:

$$e_d = \frac{1}{\omega_o}\frac{d\psi_d}{dt} - \frac{\omega}{\omega_0}\psi_q - R_a i_d \tag{2.1}$$

$$e_q = \frac{1}{\omega_o}\frac{d\psi_q}{dt} + \frac{\omega}{\omega_0}\psi_d - R_a i_q \tag{2.2}$$

The rotor equations:

$$e_{fd} = \frac{1}{\omega_o}\frac{d\psi_{fd}}{dt} + R_{fd} i_{fd} \tag{2.3}$$

$$0 = \frac{1}{\omega_0}\frac{d\psi_{1d}}{dt} + R_{1d} i_{1d} \tag{2.4}$$

$$0 = \frac{1}{\omega_0}\frac{d\psi_{1q}}{dt} + R_{1q} i_{1q} \tag{2.5}$$

$$0 = \frac{1}{\omega_0}\frac{d\psi_{2q}}{dt} + R_{2q} i_{2q} \tag{2.6}$$

The stator flux linkage equations:

$$\psi_d = -L_d i_d + L_{ad} i_{fd} + L_{ad} i_{1d} \tag{2.7}$$

$$\psi_q = -L_q i_q + L_{aq} i_{1q} + L_{aq} i_{2q} \tag{2.8}$$

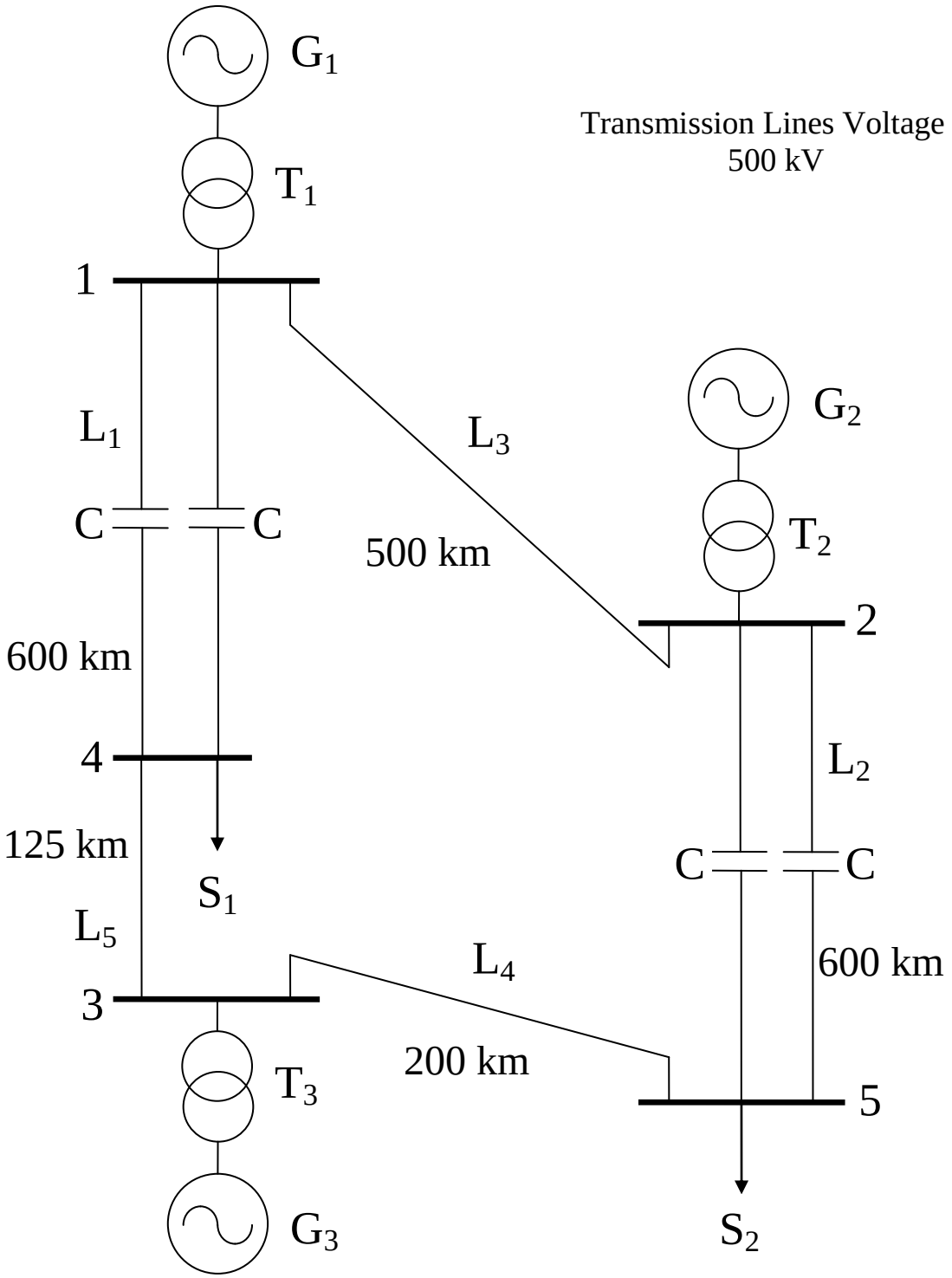


Figure 2.1: System under study.

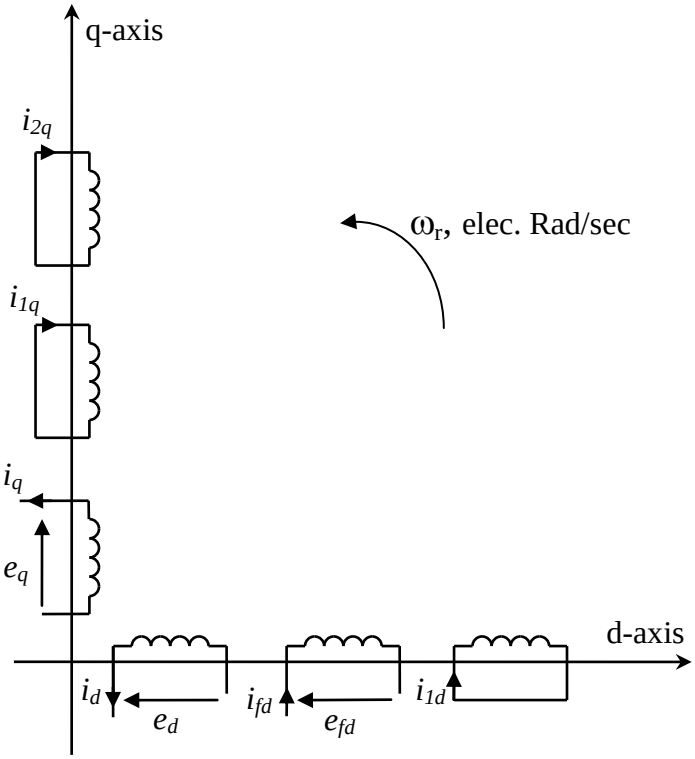


Figure 2.2: Modeling of the synchronous machine in the d-q reference frame.

The rotor flux linkage equations:

$$\psi_{fd} = L_{ffd} i_{fd} + L_{ad} i_{1d} - L_{ad} i_d \tag{2.9}$$

$$\psi_{1d} = L_{ad} i_{fd} + L_{11d} i_{1d} - L_{ad} i_d \tag{2.10}$$

$$\psi_{1q} = L_{11q} i_{1q} + L_{aq} i_{2q} - L_{aq} i_q \tag{2.11}$$

$$\psi_{2q} = L_{aq} i_{1q} + L_{22q} i_{2q} - L_{aq} i_q \tag{2.12}$$

The air-gap torque equation:

$$T_{ELEC} = \psi_d i_q - \psi_q i_d \tag{2.13}$$

The overall differential equations which describe the transient performance of the synchronous machine are given by the following matrix equation:

$$\left[\frac{dX_{syn}}{dt}\right] = [At_{syn}][X_{syn}] + [Bt_{syn}]\begin{bmatrix} V_{td} \\ V_{tq} \\ e_{fd} \end{bmatrix} \tag{2.14}$$

where

$$\left[X_{syn}\right] = [i_d \quad i_q \quad i_{fd} \quad i_{1q} \quad i_{1d} \quad i_{2q}]^T$$

$$\left[At_{syn}\right] = [L]^{-1}[Qt]$$

$$\left[Bt_{syn}\right] = [L]^{-1}[Rt]$$

$$[L] = \begin{bmatrix} -L_d & 0 & L_{ad} & 0 & L_{ad} & 0 \\ 0 & -L_q & 0 & L_{aq} & 0 & L_{aq} \\ -L_{ad} & 0 & L_{ffd} & 0 & L_{ad} & 0 \\ 0 & -L_{aq} & 0 & L_{11q} & 0 & L_{aq} \\ -L_{ad} & 0 & L_{ad} & 0 & L_{11d} & 0 \\ 0 & -L_{aq} & 0 & L_{aq} & 0 & L_{22q} \end{bmatrix} \tag{2.15}$$

$$[Qt] = \begin{bmatrix} \omega_0 R_a & -\omega L_q & 0 & \omega L_{aq} & 0 & \omega L_{aq} \\ \omega L_d & \omega_0 R_a & -\omega L_{ad} & 0 & -\omega L_{ad} & 0 \\ 0 & 0 & -\omega_0 R_{fd} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega_0 R_{1q} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\omega_0 R_{1d} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\omega_0 R_{2q} \end{bmatrix}$$

$$[Rt] = \begin{bmatrix} \omega_0 & 0 & 0 \\ 0 & \omega_0 & 0 \\ 0 & 0 & \omega_0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

here, the superscript $"T"$ means matrix transpose.

The synchronous machine swing equation can be written as:

$$\frac{2H}{\omega_0}\frac{d\omega}{dt} = T_{MECH} - T_{ELEC} \tag{2.16}$$

$$\frac{d\delta}{dt} = \omega - \omega_0 \tag{2.17}$$

In the above two equations (2.16 and 2.17), ω is in radians per second, the inertia constant H is in seconds, and the load angle δ is in radians, ω_o is the synchronous frequency (377 rad/sec) and the mechanical and electrical torques T_{MECH} and T_{ELEC} are in per unit.

In developing the equations of multi-machine systems, the equations of each synchronous machine expressed in its own d-q reference frame which rotates with its rotor must be expressed in a common reference frame. Usually, a reference frame rotating at synchronous speed is used as the common reference. Axis transformation equations are used to transform between the individual machine (d-q) reference frames and the common (R-I) reference frame [17].

2.3.2 Modeling of the transmission line

A series capacitor-compensated transmission line may be represented by the *RLC* circuit shown in Figure 2.3 [18]. In the voltage phasor diagram shown in Figure 2.4, the rotor angle δ is the angle (in elec. rad) by which the q-axis leads the reference voltage V_b. The differential equations for the circuit elements, after applying Park's transformation [18], can be expressed in the d-q reference frame by the following matrix expressions.

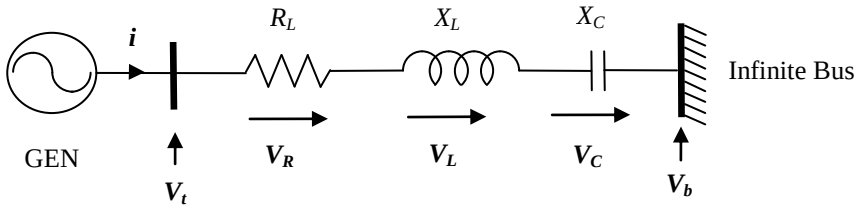


Figure 2.3: A series capacitor-compensated transmission line.

The voltage across the resistance:

$$\begin{bmatrix} V_{Rd} \\ V_{Rq} \end{bmatrix} = \begin{bmatrix} R_L & 0 \\ 0 & R_L \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.18}$$

The voltage across the inductance:

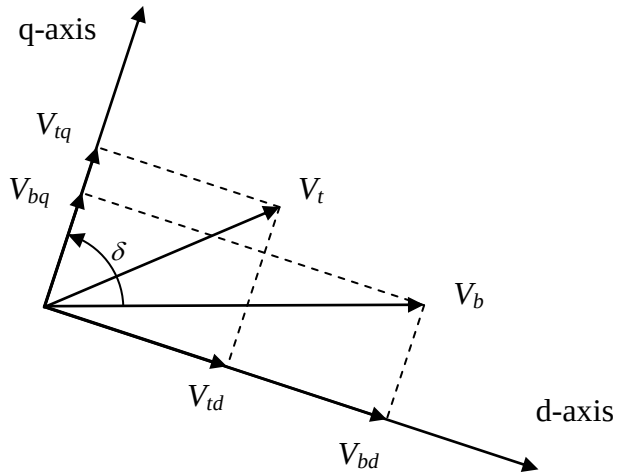


Figure 2.4: Voltage phasor diagram.

$$\begin{bmatrix} V_{Ld} \\ V_{Lq} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{\omega}{\omega_0} X_L \\ \frac{\omega}{\omega_0} X_L & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \frac{X_L}{\omega_o} & 0 \\ 0 & \frac{X_L}{\omega_o} \end{bmatrix} \begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} \tag{2.19}$$

The voltage across the capacitor:

$$\begin{bmatrix} \frac{dV_{Cd}}{dt} \\ \frac{dV_{Cq}}{dt} \end{bmatrix} = \begin{bmatrix} \omega_0 X_C & 0 \\ 0 & \omega_0 X_C \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} V_{Cd} \\ V_{Cq} \end{bmatrix} \tag{2.20}$$

The overall equations of the transmission line can be written as

$$\begin{bmatrix} \frac{dV_{Cd}}{dt} \\ \frac{dV_{Cq}}{dt} \\ V_{td} \\ V_{tq} \end{bmatrix} = [Att] \begin{bmatrix} V_{Cd} \\ V_{Cq} \end{bmatrix} + [Rt1] \begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} + [Rt2] \begin{bmatrix} i_d \\ i_q \end{bmatrix} + [Btt][V_b] \tag{2.21}$$

where

$$[Att] = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$[Rt1] = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{X_L}{\omega_o} & 0 \\ 0 & \frac{X_L}{\omega_o} \end{bmatrix}$$

$$[Rt2] = \begin{bmatrix} \omega_0 X_C & 0 \\ 0 & \omega_0 X_C \\ R_L & -\frac{\omega}{\omega_0} X_L \\ \frac{\omega}{\omega_0} X_L & R_L \end{bmatrix} \tag{2.22}$$

$$[Btt] = \begin{bmatrix} 0 \\ 0 \\ \sin\delta \\ \cos\delta \end{bmatrix}$$

2.3.3 Excitation system

The block diagram representation of the excitation system used in this study is shown in Figure 2.5, and the corresponding data are given in Appendix A [18].

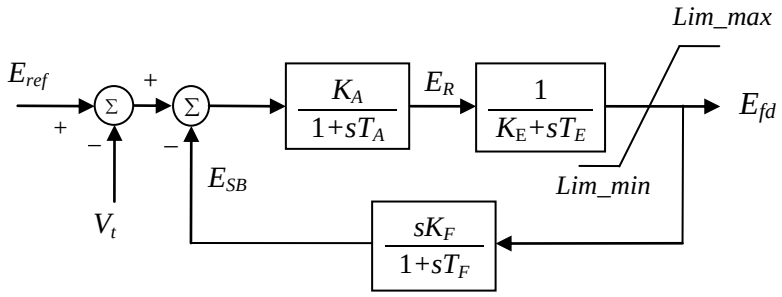


Figure 2.5: Block diagram of the excitation system.

Utilizing the relationship between the excitation system output voltage and the field voltage given by $E_{fd} = \frac{L_{ad}}{R_{fd}} e_{fd}$, the state-space equation of the excitation system can be derived from its block diagram and is given by

$$\left[\frac{dX_v}{dt}\right] = [At_v][X_v] + [Bt_v]\begin{bmatrix} V_t \\ V_{ref} \end{bmatrix} \tag{2.23}$$

where,

$$[X_v] = [e_{fd} \quad E_R \quad E_{SB}]^T$$

$$[At_v] = \begin{bmatrix} -\frac{K_E}{T_E} & \frac{1}{T_E}\frac{R_{fd}}{L_{ad}} & 0 \\ 0 & -\frac{1}{T_A} & -\frac{K_A}{T_A} \\ -\frac{K_E K_F}{T_E T_F}\frac{L_{ad}}{R_{fd}} & \frac{K_F}{T_F T_E} & -\frac{1}{T_F} \end{bmatrix} \tag{2.24}$$

$$[Bt_v] = \begin{bmatrix} 0 & 0 \\ -\frac{K_A}{T_A} & \frac{K_A}{T_A} \\ 0 & 0 \end{bmatrix}$$

2.3.4 Modeling of the transformer

The three-phase transformer is constructed by using three single-phase transformers connected in Delta (LV side) / Y grounded (HV side). The transformer leakage and magnetizing reactances as well as the winding resistances and core loss are represented in the model.

2.3.5 Modeling of system loads

The system loads are modeled in these studies by constant impedances. The formula, which is used in calculating the load impedances, is given by [19]:

$$Z_{Load} = \frac{|V_{Load}|^2}{P_{Load} - jQ_{Load}} \tag{2.25}$$

where,

Z_{Load} = load impedance.
V_{Load} = load voltage.
P_{Load} = load real power.
Q_{Load} = load reactive power.

2.4 A Sample Case Study

In the studies conducted in this thesis, the ElectroMagnetic Transients Program (EMTP-RV) is used for modeling the various system components and producing the time-domain simulation results [20]. Due to the initialization process in the EMTP-RV, simulation results will be displayed starting at time equal four seconds. Moreover, faults are assumed to occur at t = 5 seconds.

Figure 2.6 shows the power flow results for the bus voltages and the line real power flows of the system under study. Figure 2.7 shows the transient time responses of the generator load angles and speeds (measured with respect to the load angle and speed of generator 1), the bus voltages, and the real power flows in the transmission lines during and after clearing a three-cycle, three-phase fault at the middle of transmission line L_3. The following observations can be made from examining these two figures:

1. The power flow results show heavy power transfers along the two compensated lines L_1 and L_2.
2. The system is stable after fault clearing. The generator load angles and speeds reach steady states. The bus voltages drop immediately at the instant of fault inception but recover after fault clearing.
3. The low frequency oscillations in the generator load angles and speeds are poorly damped.
4. The system under study has three generators; therefore, it has two natural modes of oscillations [21]. In general, synchronous machines respond to disturbances by complex oscillations that involve several natural frequencies, but a particular machine or group of coherent machines may tend to favor one mode over all others [2]. This is the case for generators 2 and 3. As it can be seen from the load angle responses of these two generators, measured with respect to the load angle of generator 1 (Figure 2.7), generators 2 and 3 tend to oscillate at a single frequency (approximately 1.4 Hz).

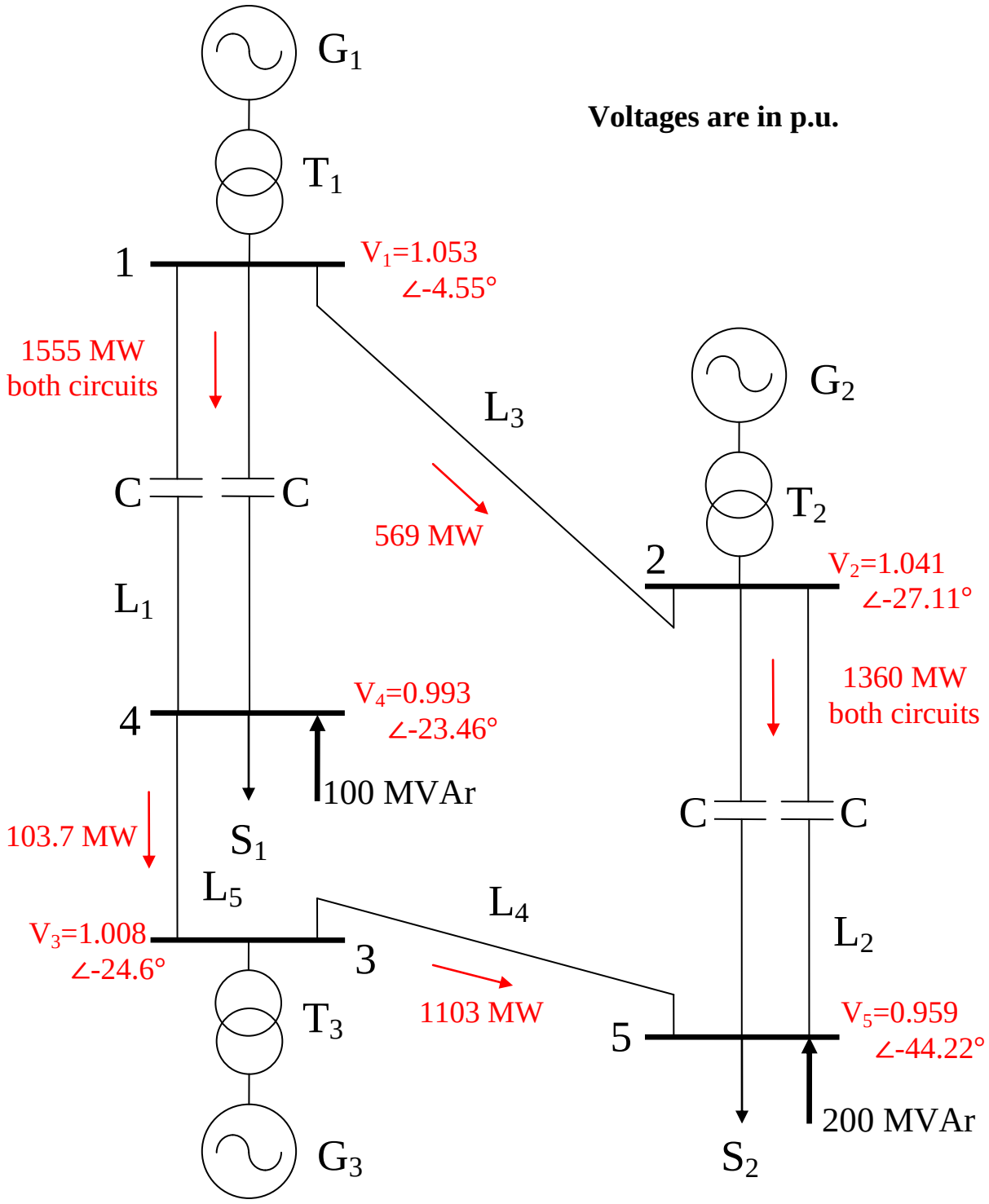


Figure 2.6: Power flow results of bus voltages and line real power flows of the system under study.

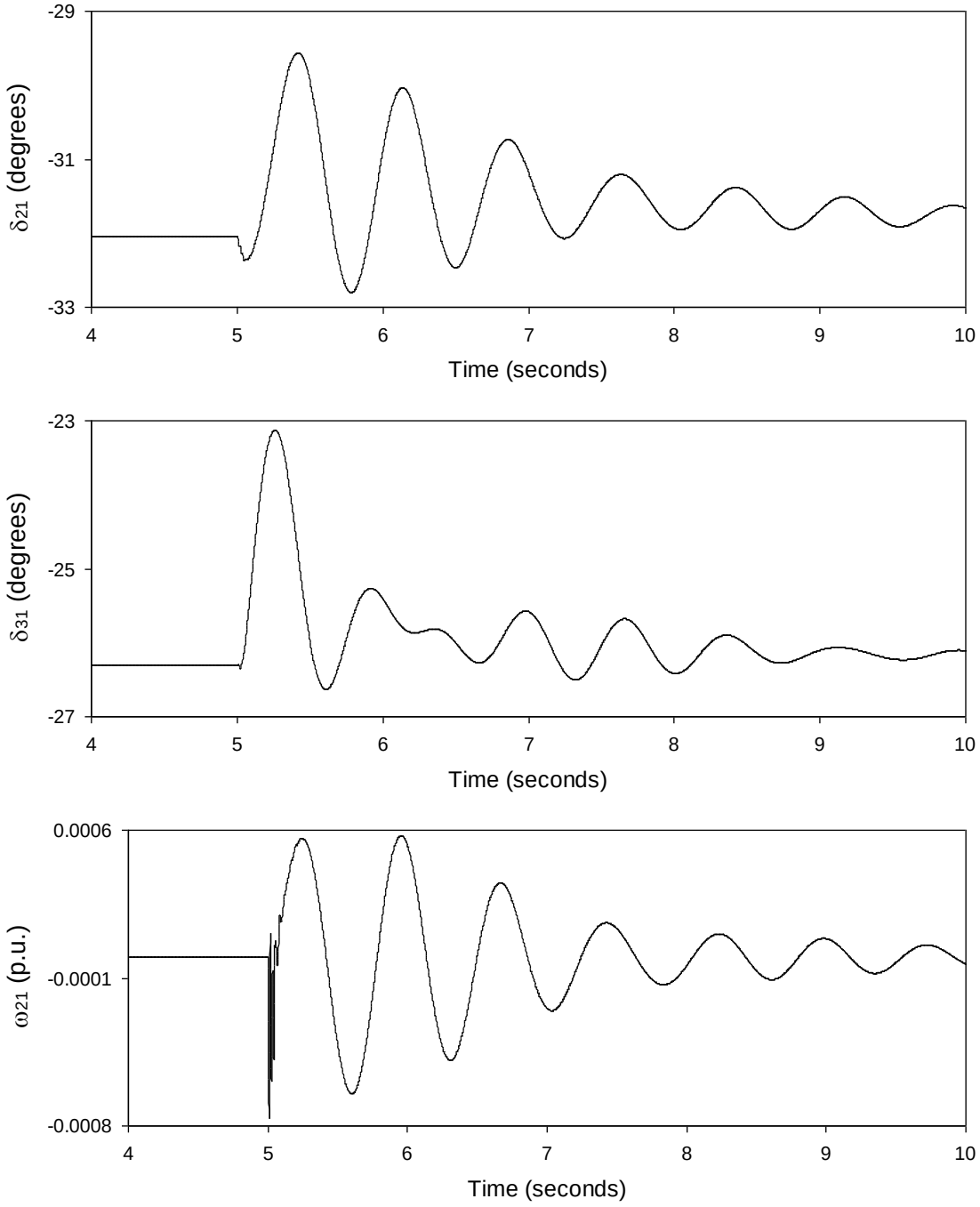


Figure 2.7: Transient time responses of the power system during and after clearing a three-cycle, three-phase fault at the middle of transmission line L_3.

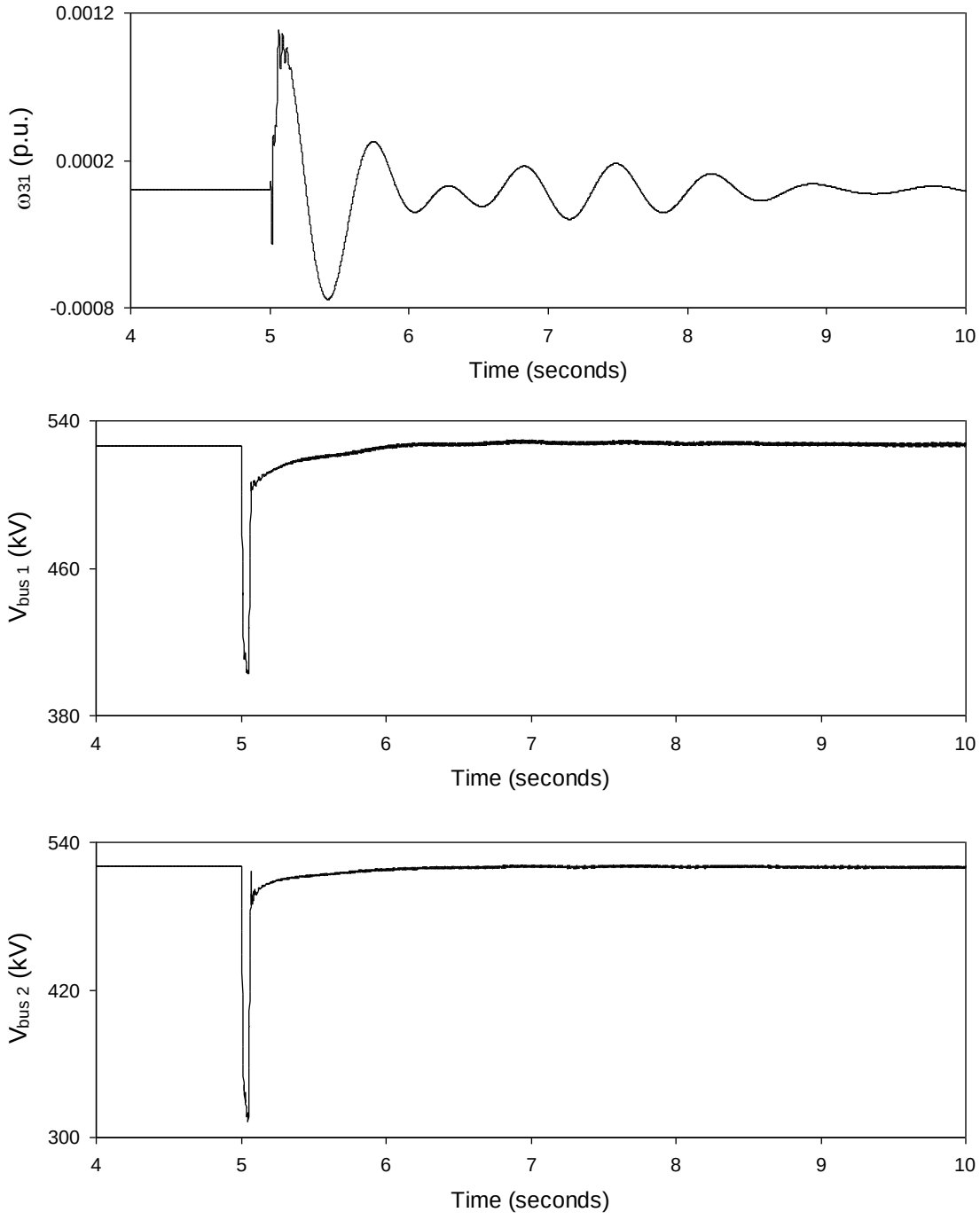
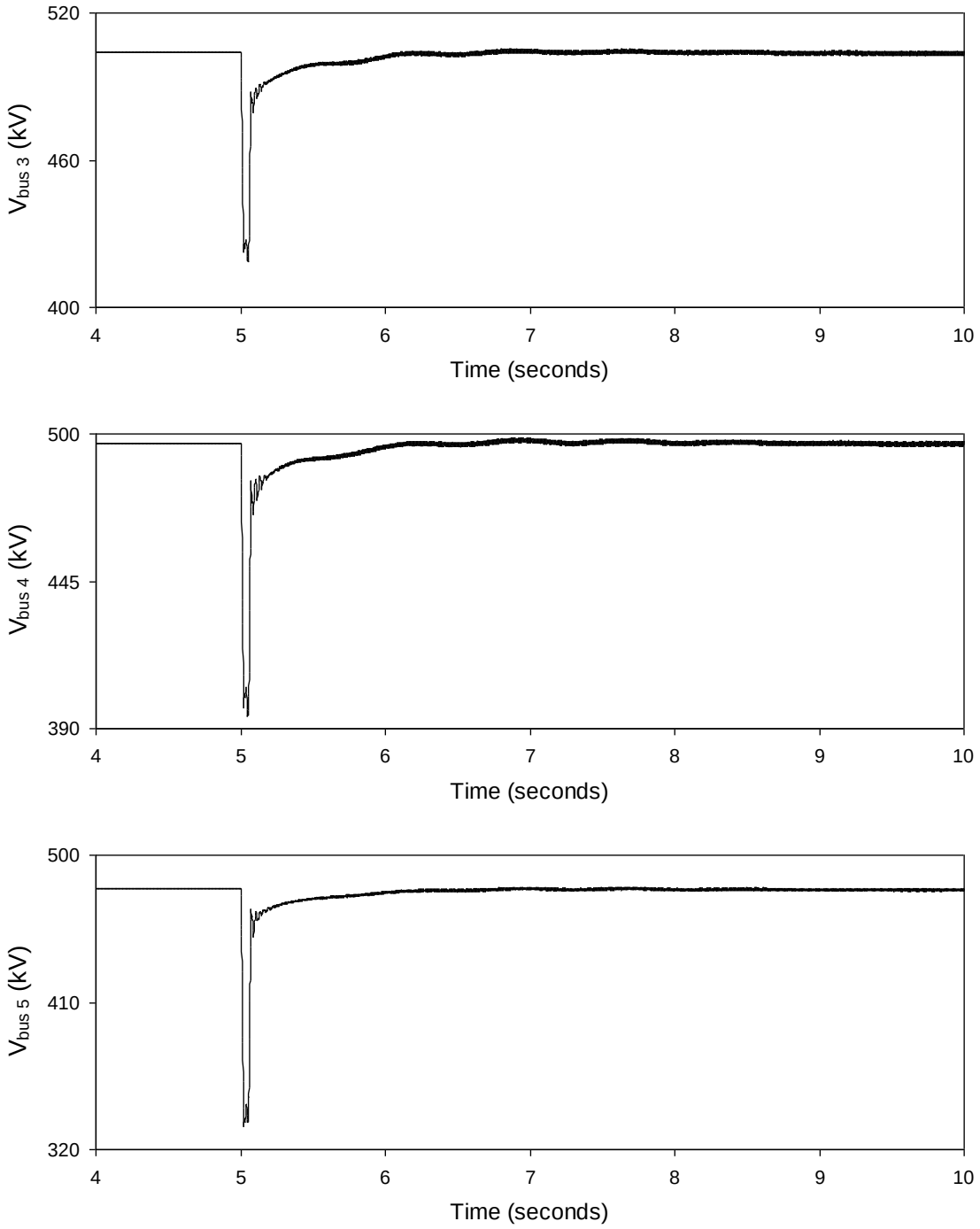


Figure 2.7: continued.



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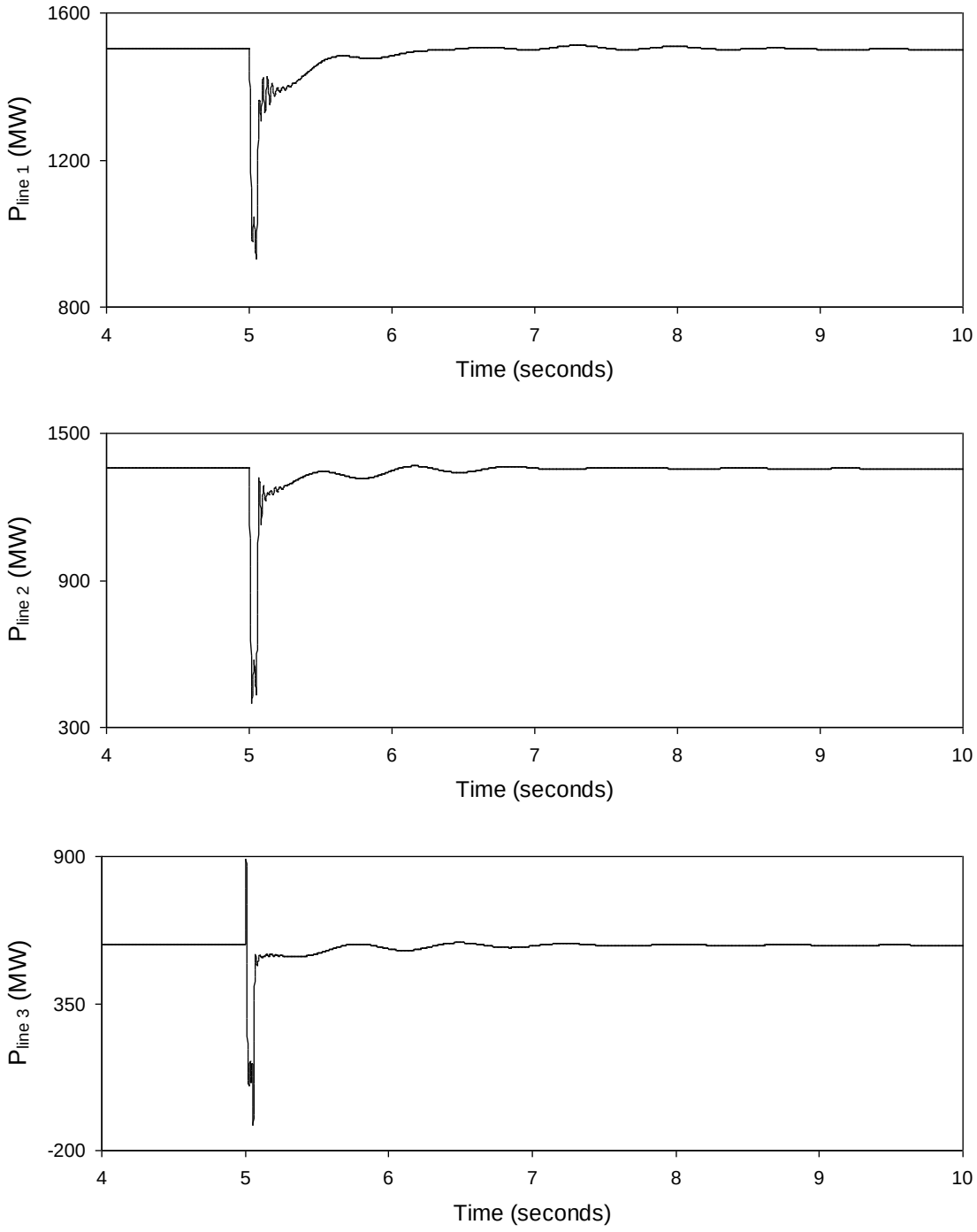


Figure 2.7: continued.

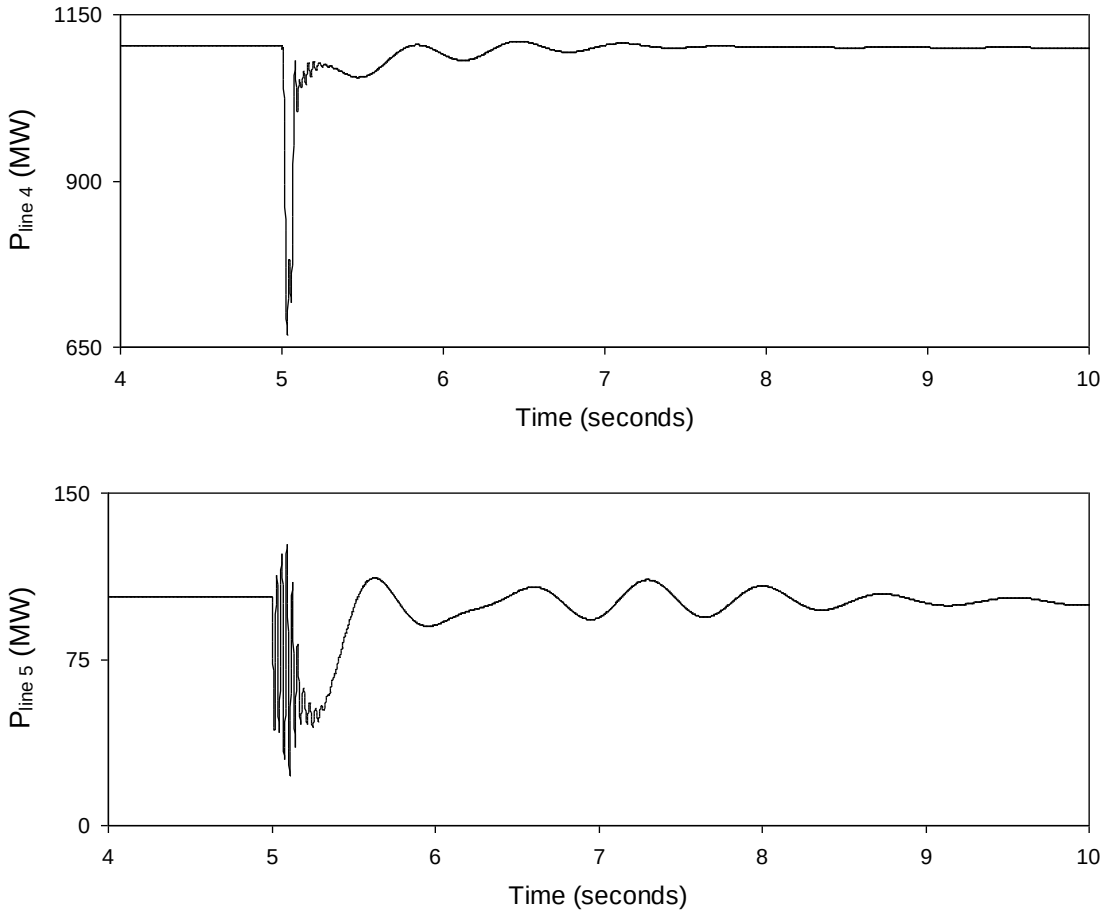


Figure 2.7: continued.

2.5 Summary

This chapter introduces the system used for the studies reported in this thesis and presents the mathematical models of its various components. A digital time-domain simulation of a case study of the system during a three-phase fault is also presented and some observations are noted.

Chapter 3

THE STATIC SYNCHRONOUS SERIES COMPENSATOR AND MODELING OF THE SINGLE-PHASE-SSSC

3.1 General

Static Synchronous Series Compensator is a series-connected converter type FACTS device. It injects a controllable voltage in series with a transmission line at the fundamental frequency by using a solid-state voltage source converter with a coupling transformer. This injected voltage is a nearly-sinusoidal ac voltage with variable magnitude and phase angle. The quadrature component of the injected voltage can be leading or lagging the line current by 90° such that the reactive power is absorbed or generated. This provides both inductive and capacitive compensation. On the other hand, the component of the injected voltage in phase with the line current enables the SSSC to exchange active power and provide resistive compensation. The resistive compensation is very beneficial when it comes to the power oscillation damping [22]. These reactive and resistive compensations influence the power flow in the transmission line.

3.2 Concept of Series Capacitive Compensation

The intention behind series capacitive compensation is to reduce the total effective series impedance between the two ends of a transmission line. The reactance of the series compensating capacitor cancels a portion of the actual line inductive reactance, thus, the effective reactance is reduced and, in turn, this escalates the transmittable power transfer of the line.

Consider a simple two-machine power system model without and with a series capacitor compensation and the corresponding phasor diagrams as shown in Figure 3.1. In this model, it is

assumed for simplicity that the transmission line resistance is negligible and, therefore, the line is represented by an inductive reactance. Moreover, it is assumed that the machines at both ends are represented by as constant amplitude sinusoidal voltages at synchronous frequency. Figure 3.1(b) shows that the series capacitor provides a lagging quadrature voltage with respect to the line current and this capacitive voltage drop opposes the leading voltage drop across the inductor. It can be observed from Figure 3.1(b) that the current and, in turn, the power flow increases in the system.

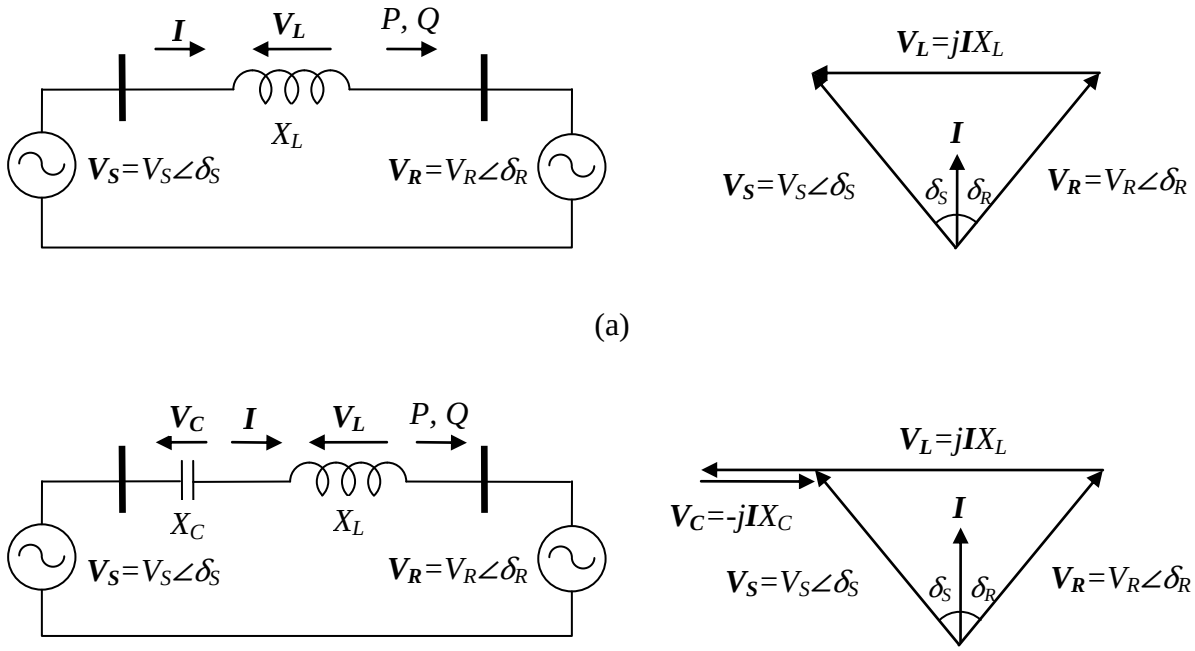


Figure 3.1: A schematic diagram of a simple two-machine power system and its vector diagrams: (a) without series compensation, (b) with series capacitor compensation.

The active (real) power at the receiving-end bus for the uncompensated system in Figure 3.1(a) is given by

$$P = \frac{V_S V_R}{X_L}\sin(\delta_S - \delta_R) = \frac{V^2}{X_L}\sin\delta \tag{3.1}$$

where V_S and V_R are the magnitudes of the sending and receiving end voltages respectively, (it is assumed that $V = V_S = V_R$), δ (is called the load angle) is the angle between the sending and receiving end voltages ($\delta = \delta_S - \delta_R$) and X_L is the transmission line inductive reactance.

For the series capacitor compensated system (Figure 3.1(b)),

$$P = \frac{V^2}{X_{eff}} \sin\delta = \frac{V^2}{(X_L - X_C)} \sin\delta = \frac{V^2}{X_L(1-\frac{X_C}{X_L})} \sin\delta = \frac{V^2}{X_L(1-k)} \sin\delta \qquad (3.2)$$

where X_C is the capacitor reactance, $X_{eff} = X_L\text{-}X_C$ is the effective reactance, and $k = \frac{X_C}{X_L}$ is the degree of series compensation ($0 \leq k < 1$).

Figure 3.2 shows the normalized active power versus the load angle of the series capacitor compensated system shown in Figure 3.1(b) as a parametric function of the degree of series capacitive compensation. It is clear that series capacitor compensation increases the transmitted power by a fixed percentage of that transmitted by the uncompensated line at a given δ and that higher power transfer is achieved by increasing the degree of the compensation.

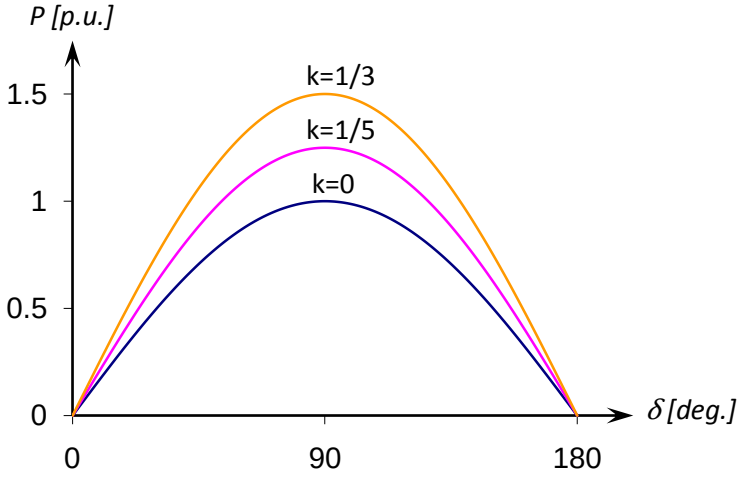


Figure 3.2: Transmitted power versus the load angle as a parametric function of the degree of series capacitive compensation.

3.3 Synchronous Voltage Source

As it is noted in Chapter 1, one of the ways to classify FACTS controllers is to group them associated with their internal circuit arrangements i.e. thyristor controlled (variable impedance) type and converter type. The basic principle of operation of the thyristor controlled type FACTS devices is to provide a variable reactive impedance to the power system and, thus, generally change the character of the system impedance. This is done by the traditional capacitors and inductors generating or absorbing necessary reactive power for the compensation and the thyristors used only for the control of the switching on and off these capacitors and inductors. On the other hand, the converter type FACTS controllers supply and absorb the reactive power

by injecting a variable ac voltage obtained from a synchronous voltage source (SVS). This approach, when compared to thyristor controlled FACTS controllers, generally provides superior performance characteristics for transmission voltage, effective line impedance, and angle control.

The SVS can be considered analogous to an ideal, rotating electromagnetic synchronous machine which produces a balanced set of sinusoidal voltages at the fundamental frequency, with controllable amplitude and phase angle: generate, or absorb reactive power to function like a synchronous condenser. This ideal machine has no inertia, its response is practically instantaneous, it does not alter the existing system impedance and it can internally generate reactive (both capacitive and inductive) power. In similar manner, SVS can be operated with a relatively small dc storage capacitor in a self-sufficient manner to exchange reactive power with the ac system. Furthermore, it can exchange real power with the ac system if it is coupled to an appropriate electric dc energy source or storage that can supply or absorb the power it supplies to, or absorbs from the ac system [8].

Figure 3.3 shows a functional representation of a SVS (series-connected here) which is composed of the voltage-sourced converter (VSC), a coupling transformer, an optional energy source and the control device. The references (the desired compensating reactive power Q_{ref} and active power P_{ref} or the desired compensating reactive impedance X_{ref} and resistance R_{ref}) define the amplitude V and phase angle φ of the generated output voltage necessary to exchange the desired reactive and active power at the ac output. If the SVS is operated for only reactive power exchange (real power exchange is not required), then P_{ref} (or R_{ref}) is set to zero and the SVS becomes a self-sufficient reactive power source like an ideal synchronous condenser and the optional external energy source or storage equipment is removed.

All the potential operating modes of the SVS at the steady-state are shown in Figure 3.4(a). It operates mainly to supply only reactive output power (capacitive compensation), hence, the optional external energy source device is replaced a fixed capacitor to supply the compensating reactive power and the external dc current becomes zero as shown Figure 3.4(b). Here, it is assumed that all SVS losses are neglected, therefore, $\boldsymbol{V}_{inj}$ is lagging the line current by 90 degrees. In practice, it is lagged a bit further to replenish its losses and keep the capacitor voltage at the desired constant level. In that case, the SVS absorbs a small amount of active power from the transmission system.

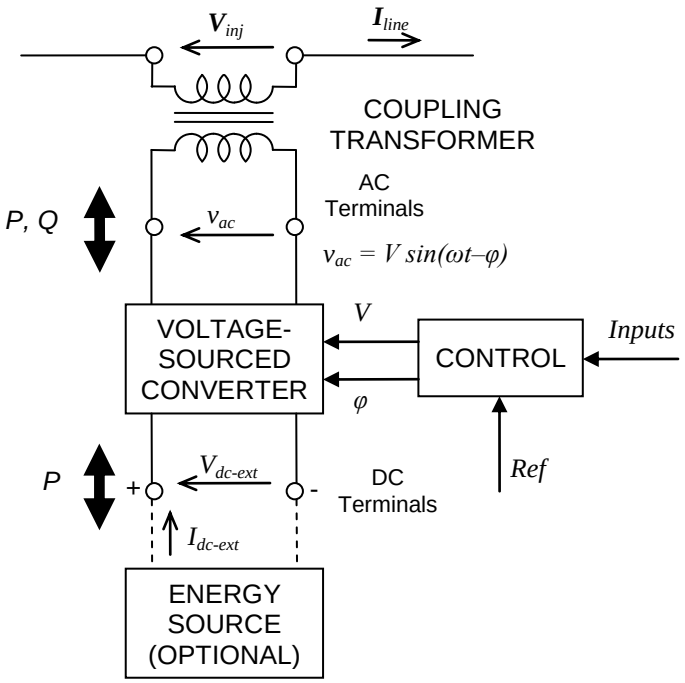


Figure 3.3: Functional representation of the SVS based on a voltage-sourced converter (VSC).

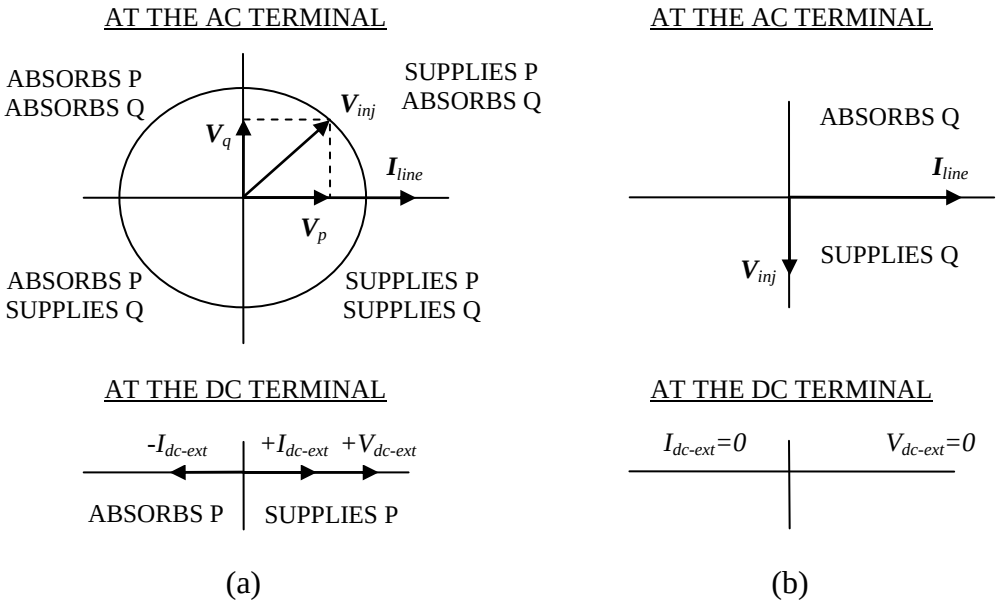


Figure 3.4: Possible steady-state operating modes and power exchange diagrams for the SVS.

3.4 Static Synchronous Series Compensator (SSSC)

The SVS-based series compensator, called Static Synchronous Series Compensator (SSSC) was proposed by Gyugyi in 1989 within the concept of using converter-based technology uniformly for shunt and series compensation as well as for transmission angle control [9]. The concept of using the SVS for series reactive compensation is based on the fact that SVS injects an ac voltage with the controllable magnitude and angle into the transmission line by being independent of the line current so it can rapidly change the effective reactance between the two ends of the transmission line and the power flow, whereas the compensating voltage is dependent on the line current in the series capacitor compensation case.

In the case of series capacitor compensation, the output voltage lags the line current by 90 degrees. However, the output voltage of the SVS can be reversed by a simple control action to make it lead or lag the line current by 90 degrees.

A generalized expression for the injected voltage, $\boldsymbol{V}_{SVS}$, can simply be written as

$$\boldsymbol{V}_{SVS} = \pm \boldsymbol{j} V_{SVS}(\zeta) \frac{\boldsymbol{I}}{I} \tag{3.3}$$

where $V_{SVS}(\zeta)$ is the magnitude of the injected compensating voltage by SVS ($0 \leq V_{SVS}(\zeta) \leq V_{SVS\text{-}max}$), ζ is a chosen control parameter, and $\boldsymbol{I}$ is the line current. The series reactive compensation scheme, using a switching power converter (voltage-sourced converter) as a synchronous voltage source to produce a controllable voltage in quadrature with the line current as defined by Equation (3.3) is, per IEEE and CIGRE definition, termed the *Static Synchronous Series Compensator (SSSC)* [9].

Equation (3.3) can be re-written for the SSSC as

$$\boldsymbol{V}_{SSSC} = \pm \boldsymbol{j} V_{SSSC}(\zeta) \frac{\boldsymbol{I}}{I}. \tag{3.4}$$

The proposed definition for the SSSC by IEEE's FACTS Terms and Definitions Task Force of the FACTS Working Group of the DC and FACTS Subcommittee is as follows: ***Static Synchronous Series Compensator (SSSC):*** *A static, synchronous generator operated without an external electric energy source as a series compensator whose output voltage is in quadrature with, and controllable independently of, the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the*

transmitted electric power . The SSSC may include transiently rated energy storage or energy absorbing devices to enhance the dynamic behavior of the power system by additional temporary real power compensation, to increase or decrease momentarily, the overall real (resistive) voltage drop across the line [23].

Figure 3.5 illustrates the different operating modes at steady-state for an SSSC installed in the simple two-machine power system model of Figure 3.1(a). The no compensation mode of operation of the SSSC ($\boldsymbol{V}_{SSSC} = 0$) is shown in Figure 3.5(b). The capacitive compensation mode is shown in Figure 3.5(c) where, as a result of the SSSC injected voltage $\boldsymbol{V}_{SSSC} = -\boldsymbol{j}V_{SSSC}(\zeta)\frac{\boldsymbol{I}}{I}$, the effective inductive reactance between the two buses is decreased and the line current is increased. This results in increasing the transmitted power. Figure 3.5(d) shows the SSSC inductive mode of operation where the transmitted power is decreased due to the injection of $\boldsymbol{V}_{SSSC} = \boldsymbol{j}V_{SSSC}(\zeta)\frac{\boldsymbol{I}}{I}$.

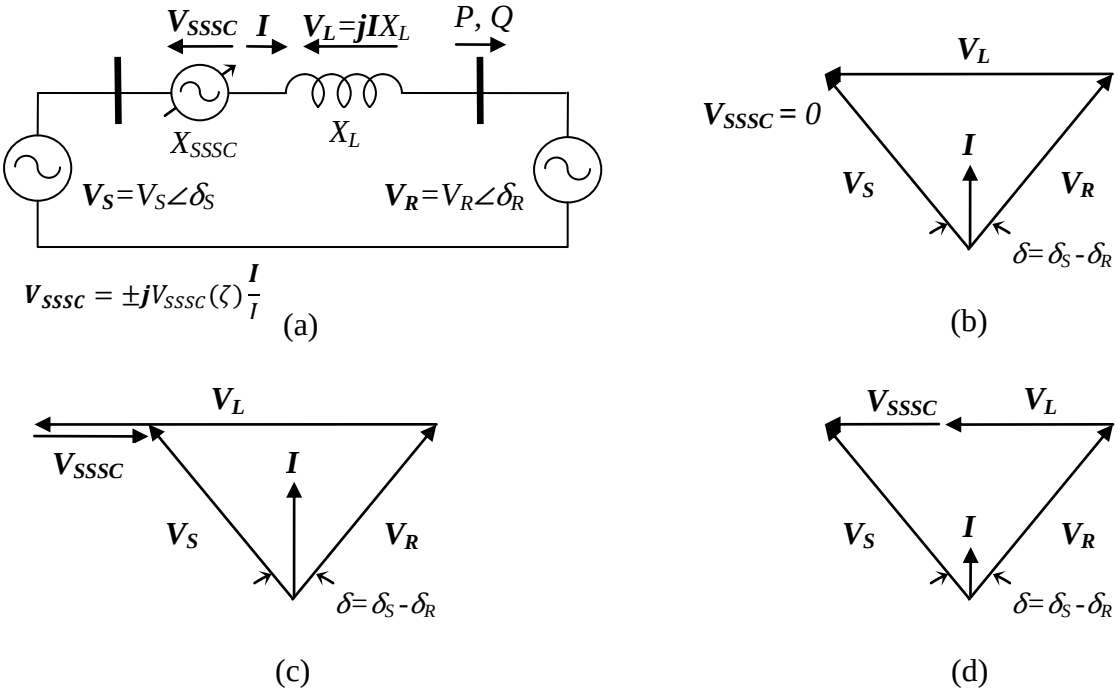


Figure 3.5: SSSC operating modes in a two-machine power system and the phasor diagrams (b) no compensation, (c) capacitive compensation, (d) inductive compensation.

Since the SSSC injects the variable compensating voltage in series by controlling the magnitude of the voltage, irrespective of the line current, the transmitted power *P* versus the load

angle δ becomes a parametric function of the injected voltage, $V_{SSSC}(\zeta)$, and it can be expressed for a two-machine system as follows

$$P = \frac{V^2}{X_L}\sin\delta + \frac{V}{X_L}V_{SSSC}(\zeta)\cos\frac{\delta}{2}. \tag{3.5}$$

The normalized power P versus angle δ plots as a parametric function of $V_{SSSC}(\zeta)$ are shown in Figure 3.6. For comparison, $V_{SSSC}(\zeta)$ is chosen to give the same maximum power as the series capacitor compensation with the corresponding k in Figure 3.2.

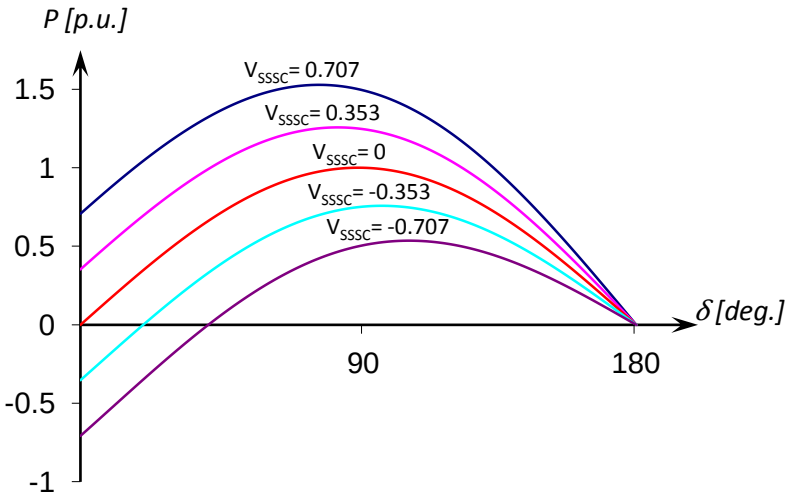


Figure 3.6: Transmitted power versus load angle provided by the SSSC as a parametric function of the degree of series compensating (injected) voltage.

The comparison of the corresponding plots in Figures 3.2 and 3.6 clearly shows that the series capacitor increases the transmitted power by a fixed *percentage* of that transmitted by the uncompensated line at a given δ and, by contrast, the SSSC can increase it by a fixed *fraction* of the maximum power transmittable by uncompensated line, independent of δ, in the important operating range of $0 \leq \delta \leq \pi/2$ [9]. The SSSC has also a capability to decrease the transmitted power by changing the polarity of the injected voltage whereas the series capacitor compensation does not have such a feature.

3.5 Hybrid Compensation Scheme [9]

The SSSC can provide capacitive or inductive compensating voltage independent of the line current up to its specified current rating. Thus, the SSSC can maintain the capacitive or the inductive compensating voltage in the face of changing the line current theoretically in the total

operating range of zero to I_{max}, as illustrated in Figure 3.7(a). (The practical minimum line current is that at which the SSSC can still absorb enough real power from the line to replenish its losses). The VA rating of the SSSC (solid-state converter and coupling transformer) is simply the product of the maximum line current (at which compensation is still desired) and the maximum series compensating voltage is $VA=I_{max}V_{SSSCmax}$. In practical applications, I_{max} may be separately defined for the rated maximum steady-state line current and for a specified short duration overcurrent.

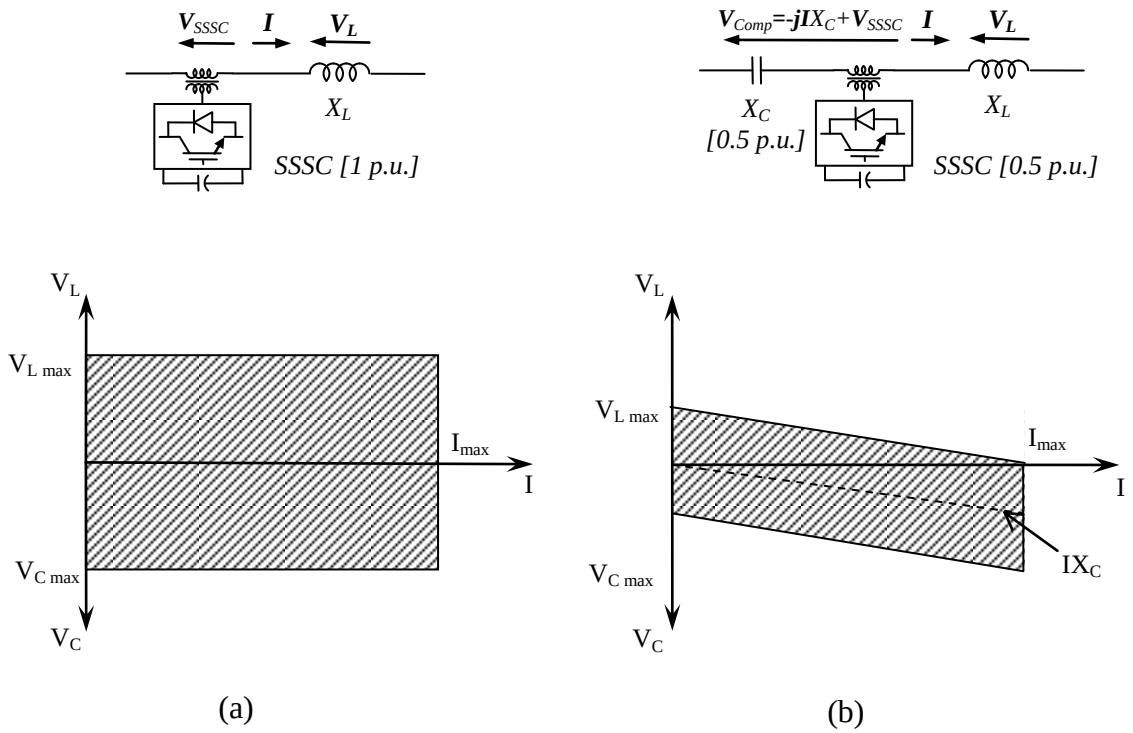


Figure 3.7: A single-line representation of (a) an SSSC alone and (b) a hybrid compensation scheme consisting of an SSSC and a fixed capacitor, and the corresponding attainable V-I (compensating voltage and line current) characteristics.

It is seen in Figure 3.7(a) that an SSSC of 1.0 p.u. VA rating covers a control range corresponding to 2.0 p.u. compensating VARs, that is, the control range is continuous from -1.0 p.u. (capacitive) VARs to +1.0 p.u. (inductive) VARs. In many practical applications, only capacitive series line compensation is required. In these applications, as well as in those which already use or plan to use series capacitors a part of the overall series compensation scheme, the SSSC may be combined cost effectively with a fixed capacitor (FC), as illustrated in Figure 3.7(b), where an SSSC of 0.5 p.u. The injected voltage versus line current characteristics of

SSSC + FC arrangement is shown in Figure 3.7(b). The VA rating is combined with a fixed capacitor of 0.5 p.u. VA rating to form a continuously controllable overall series compensator with a maximum compensating range of zero to 1.0 p.u. capacitive. This compensation scheme from the standpoints of major component (converter and fixed capacitor) ratings and operating losses is extremely advantageous, in spite of the fact that the fixed capacitor produces a compensating voltage that is proportional to the line current, and therefore, the controllable compensating voltage range of the overall compensator also becomes, to some degree, a function of the line current.

3.6 Hybrid Single-Phase-SSSC Compensation Scheme

The recently proposed phase imbalanced series capacitive compensation concept has been shown to be effective in enhancing power system dynamics as it has the potential of damping power swing as well as subsynchronous resonance oscillations [24], [25]. Figure 3.8 shows such a scheme for a phase imbalanced capacitive compensation. It is a *"hybrid"* series capacitive compensation where the series capacitive compensation in one phase is created using a single-phase-SSSC in series with a fixed capacitor C_c, and the other two phases are compensated by fixed capacitors C. The SSSC control is initially set such that its equivalent compensation at the power frequency combined with the fixed capacitor C_c yields a resultant compensation equal to the other two phases. Thus, the phase balance is maintained at the power frequency while at any other frequency, a phase imbalance is created. Mathematically, this can be explained as follows:

1) At the power frequency, the series reactance between buses X and Y, in Figure 3.8, in phases a, b, and c are given by:

$$\boldsymbol{X_a = X_b = \frac{1}{j\omega_0 C}} \tag{3.6}$$

$$\boldsymbol{X_c = \frac{1}{j\omega_0 C_c} - jX_{SSSCo}} \tag{3.7}$$

where $-\boldsymbol{jX_{SSSCo}}$ is the effective capacitive reactance of the SSSC at the power frequency such that $X_a=X_b=X_c$.

2) During any other frequency, f_e, including subsynchronous frequencies,

$$\boldsymbol{X_c = \frac{1}{j\omega_e C_c} - jX_{SSSCo} - j\Delta X_{SSSC}} \tag{3.8}$$

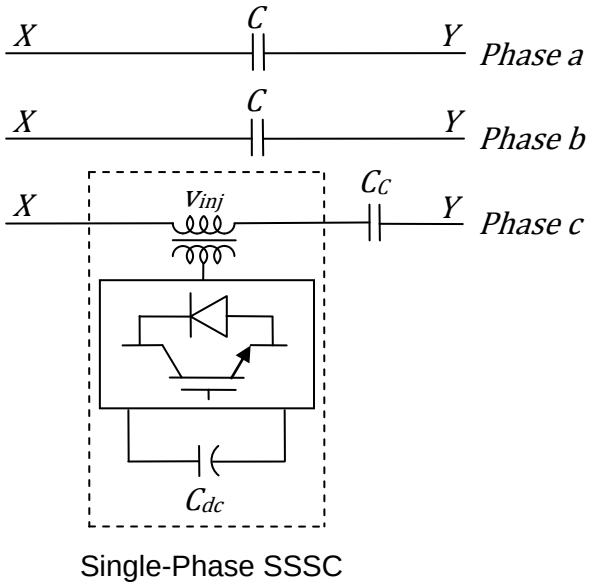


Figure 3.8: The hybrid single-phase-SSSC compensation scheme.

The first terms in Equations (3.7) and (3.8) are different because of the difference in frequency. The third term in Equation (3.8) represents the change in the effective capacitive reactance of the SSSC due to the action of the SSSC supplemental controller.

3.7 Modeling of the Single-Phase-SSSC

Figure 3.9 shows a functional model of the single-phase-SSSC. Its main components are; a dc capacitor, a single-phase voltage-sourced converter (SPVSC), a low-pass (LP) filter and a coupling transformer. The origin of the ac voltage of the SPVSC comes from the dc voltage across the dc capacitor, C_{dc}. The dc voltage is kept constant (the dc capacitor is maintained charged) at a reference value by rectified power from the ac transmission line (a small amount of real power is drawn to supply the low losses of the SPVSC). The SPVSC can be a simple single-square wave, a multi-pulse or a complex multi-level converter. The converter is operated by gate signals generated by a gate pattern generator which is controlled by the controller. The controller receives the local inputs such as line current and voltages and produces the appropriate control signal according to the desired reference values. The LP filter is used to filter out the harmonics in order to obtain the nearly-sinusoidal waveform from nonsinusoidal output of SPVSC. The coupling transformer is a step-up power transformer which is used to interconnect the SPVSC to the high voltage transmission line.

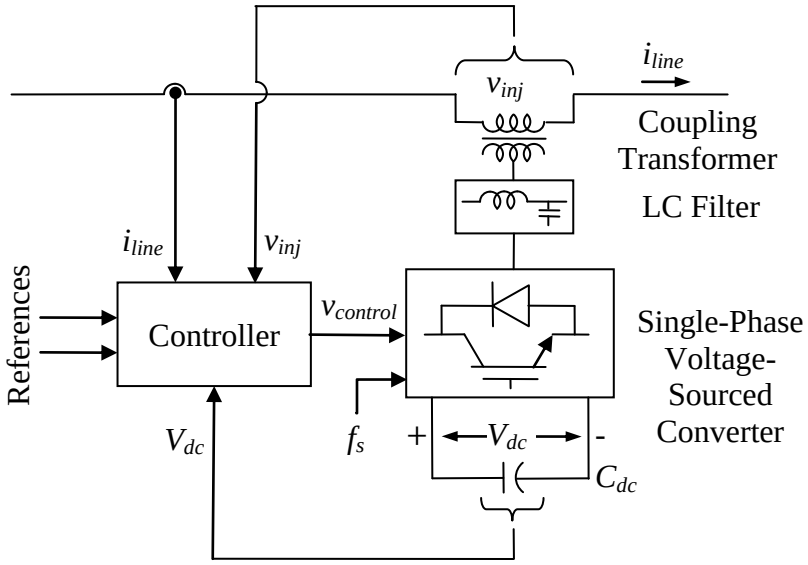


Figure 3.9: A functional model of the single-phase-SSSC.

3.8 Single-Phase Voltage-Sourced Converter

3.8.1 Operating modes of a single-phase converter

Although dc-to-ac converters are mostly called inverters because in most of the times the power flows from the dc side to the ac side, they are actually converters because the power flow is reversible. Dc-to-ac converters are used in a very wide application area ranging from residential to utility applications where the objective is to generate a sinusoidal ac output from a dc input source, in which the magnitude, the phase angle, and the frequency can be controlled. The dc input may be a battery, a fuel cell, a solar cell or other dc sources such as a rectifier.

The conceptual block diagram of a dc-ac converter is illustrated in Figure 3.10(a) where the output is filtered so that the output voltage, v_o can be considered to be sinusoidal. Since it is assumed that the load is inductive here, the output current, i_o is lagging, as shown in Figure 3.10(b). The output waveforms in Figure 3.10(b) show that during interval 1, v_o and i_o are both positive, whereas during interval 3, v_o and i_o are both negative. Therefore, during intervals 1 and 3, the instantaneous power flow p_o (= $v_o i_o$) is from the dc side to the ac side, corresponding to an inverter mode of operation. In contrast, v_o and i_o are of opposite signs during intervals 2 and 4, and, therefore, p_o flows from the ac side to the dc side of the converter, corresponding to a

rectifier mode of operation. The converter of Figure 3.10(a) must be capable of operating in all four quadrants of the v_o-i_o plane as shown in Figure 3.10(c) during each cycle of the ac output.

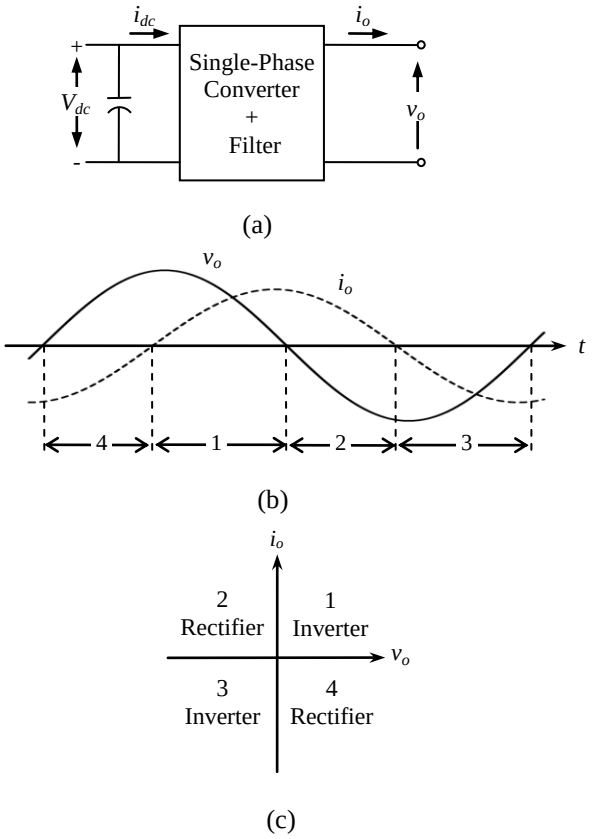


Figure 3.10: A single-phase dc-ac converter.

3.8.2 Power electronic switching elements

In converter circuits, two-quadrant switches are required. The output current is ac and hence, it is sometimes positive or negative. It can also be shown that the direct current in a converter flows in either direction and that the dc voltage does not reverse and, therefore, the switches have to be bidirectional. Moreover, they must be capable of conducting both positive and negative currents while block only positive voltage. In the case of simple rectifier circuits, only single-quadrant switches are enough because the current is allowed to flow in only one direction. Single-quadrant switches are capable of conducting currents of a single polarity and blocking voltages of a single polarity. Figures 3.11 show the operation areas of single- and two-quadrant switches in the *i*-*v* plane.

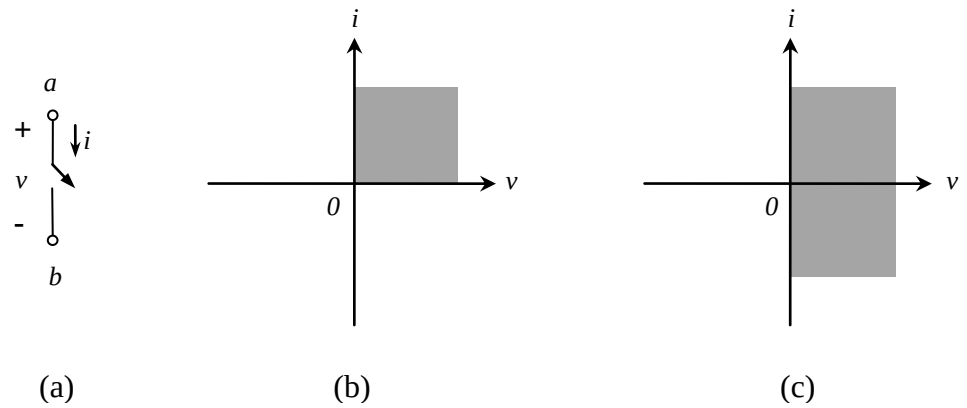


Figure 3.11: A controllable switch: (a) representation, (b) single-quadrant switch, (c) two-quadrant switch.

Figures 3.12(a) and 3.12(b) show the circuit symbol for a diode and its steady-state *i-v* characteristic. When the diode is forward biased, it begins to conduct with only a small forward voltage across it, which is on the order of 1 V. When the diode is reverse biased, only a negligibly small leakage current (I_s) flows through the device until the reverse breakdown voltage (V_{BR}) is reached. In normal operation, the reverse-bias voltage should not reach the breakdown rating (usually greater than 1000 V [26]). Figure 3.12(c) shows the idealized characteristic of a diode in which the diode is off ($i = 0$) when $v<0$ and is on ($v = 0$) when $i>0$. It can block the reverse biased voltage but not the forward biased voltage.

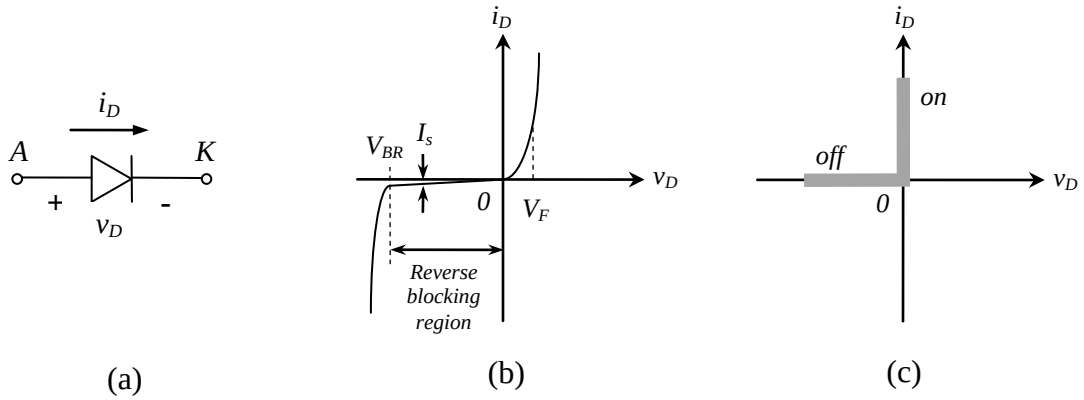


Figure 3.12: A diode: (a) symbol, (b) *i-v* characteristics, (c) idealized characteristics.

Insulated Gate Bipolar Transistor (IGBT) has progressed to become a choice in a wide range of low and medium power applications going up to several megawatts and even a few tens of megawatts. Thus, IGBT is of some importance to FACTS controllers. It operates as a

transistor with high-voltage and high-current capability and a moderate forward voltage drop during conduction. The advantage of the IGBT is its fast turn-on and turn-off so that it can be used in Pulse Width Modulation (PWM) converters operating at high frequency [9].

The circuit symbol for an IGBT and its *i-v* characteristic are shown in Figures 3.13(a) and 3.13(b) respectively. The IGBT has a high impedance gate which requires only a small amount of energy to switch the device. Like Bipolar Junction Transistor (BJT), the IGBT has a small on-state voltage even in devices with large blocking voltage ratings (for example, V_{on} is 2-3 V in a 1000-V device). Similar to the Gate-Turn-Off Thyristors (GTO), IGBTs can be designed to block negative voltage, as their idealized switching characteristic shows in Figure 3.13(c) [27]. The conducting state is determined by the a signal applied to the control terminal, Gate (G) and does not directly depend on the waveforms of *v(t)* or *i(t)* applied to terminals Collector (C) and Emitter (E) whereas diodes depend on. When the control signal causes the IGBT to be in the off state, $i = 0$, and the device is capable of blocking positive voltage $v \geq 0$. When the control signal causes the IGBT to be in the on state, $v = 0$ and the device is capable of conducting positive current $i \geq 0$.

Although the current rating of a single IGBT can be up 1200 V, 400 A, the upper limits of commercially available ratings are increasing (e.g. as high as 6500 V and 2400 A) [26]. They are used in PWM converters in which the switching frequency is up to 20 kHz, even though IGBTs have turn-on and turn-off times on the order of 1 μs [26], [27]. IGBTs may be operated in series to increase their voltage-handling capability and are also connected in parallel if one device cannot handle the load current demand.

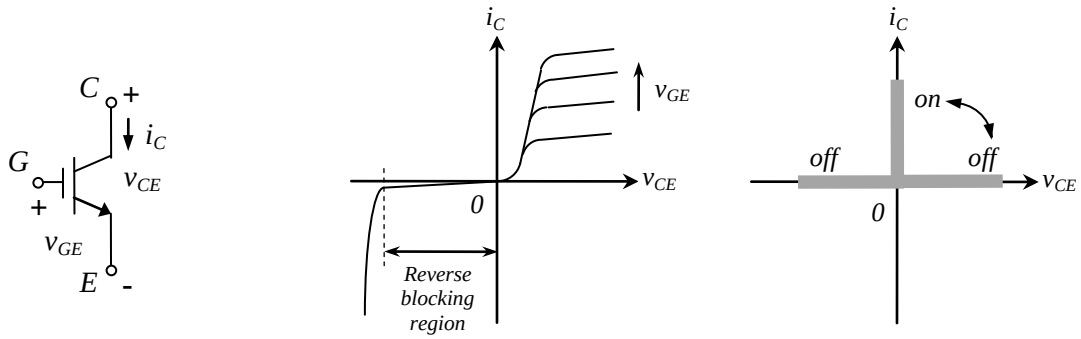
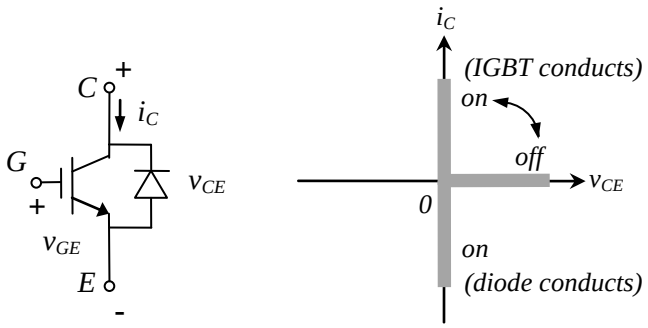


Figure 3.13: An IGBT: (a) symbol, (b) *i-v* characteristics, (c) idealized characteristics.

As it can be seen from the above descriptions, both the diode and the IGBT are single-quadrant switching elements that are not adequate for converter circuits. A current-bidirectional two-quadrant switching element can be realized using an IGBT with a diode connected in an anti-parallel manner as in Figure 3.14(a). The IGBT and the diode can be built in a monolithic integrated circuit for converters. However, for high power converters, provision of separate diodes is advantageous. In reality, there would be several IGBT-diode pair units in series for high-voltage applications [9].



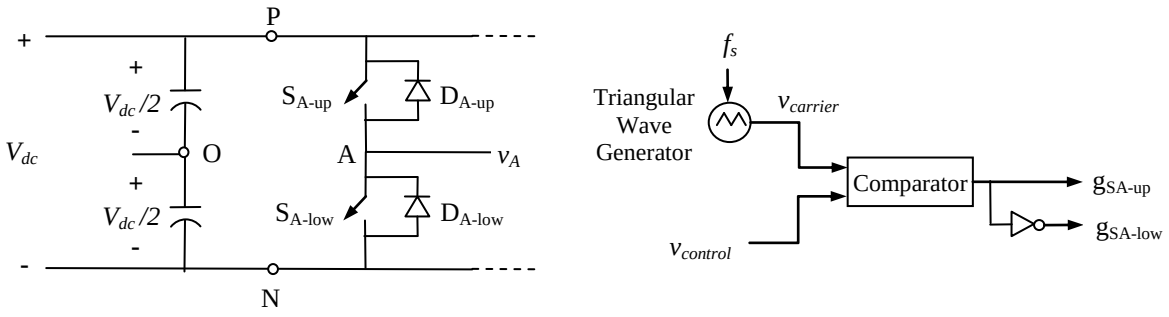
(a) (b)

Figure 3.14: A current-bidirectional two-quadrant switch: (a) implementation, (b) idealized characteristics.

3.8.3 Pulse-width modulation (PWM)

PWM creates a series of switching pulses to produce a sinusoidal fundamental component of the output voltage waveform at the desired frequency by comparing a control signal $v_{control}$ with a carrier signal, $v_{carrier}$. Figure 3.15(a) shows a one-leg of a converter (a single-phase or a three-phase converter) where the dc voltage is assumed to be constant and the output voltage v_{AO} (with a fundamental component v_{AO1}) is obtained between terminals A and O. Figure 3.15(b) shows a simple switching logic scheme that generates the corresponding gate signals. This scheme is also called in the literature the single-phase half-bridge converter.

There are various techniques to pulse-width modulate the converter switches in order to shape the desired output waveform. The commonly used techniques are; single-pulse-width modulation, multiple-pulse-width modulation, sinusoidal pulse-width modulation, modified sinusoidal pulse-width modulation and phase-displacement control [26].



(a) (b)

Figure 3.15: (a) One leg of a converter; (b) a simple switching generator scheme.

As seen in Figure 3.16(a), the control signal is a sinusoidal waveform at the fundamental frequency f_1 and the carrier signal is in a triangular waveform at which the peak magnitude $\hat{V}_{carrier}$ is kept constant at its switching frequency f_s. This technique is called the sinusoidal pulse-width modulation (SPWM). The on and off pulses to the switches correspond to the crossing points of the triangular wave with the sine wave. The negative slope of the triangular wave crossing the sine wave results in an on pulse for $S_{A\text{-}up}$ and an off pulse for $S_{A\text{-}low}$ which results in that the output voltage is $V_{dc}/2$. The positive slope of the triangular wave crossing the sine wave results in an on pulse for $S_{A\text{-}low}$ and an off pulse for $S_{A\text{-}up}$ which results in that the output voltage is $-V_{dc}/2$. With a fixed triangular wave, increasing the magnitude of the sine wave will increase the pulse width and that is, the conduction time for $S_{A\text{-}up}$ and decrease the pulse width and that is, the conduction time for $S_{A\text{-}low}$ for the positive half-cycle and vice versa for the negative half-cycle. This means that the fundamental component of the output voltage and, hence, the output ac voltage will increase with an increase in the magnitude of the control sine wave, and decrease with a decrease in the magnitude of the control sine wave. For control a sine wave peak less than the triangular wave peak, the output ac voltage varies linearly with the variation of the control sine wave magnitude.

Some basic terms related to SPWM in this thesis are given below:

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{carrier}} \tag{3.9}$$

$$m_f = \frac{f_s}{f_1} \tag{3.10}$$

where,

$\hat{V}_{control}$: Control signal peak magnitude,

$\hat{V}_{carrier}$: Carrier signal peak magnitude,

m_a : Amplitude modulation ratio or modulation index,

m_f : Frequency modulation ratio.

The m_f should be an odd integer. Choosing m_f as an odd integer results in an odd symmetry (*f(-t)=-f(t)*) as well as a half-wave symmetry (*f(t)=-f(t+T/2)*) with the time origin shown in Figure 3.16(d), which is plotted for m_f = 15. Therefore, only odd harmonics are present and the even harmonics disappear from the waveform of v_{AO} [27]. The harmonic amplitude spectrum for $m_a = 0.8$ and $m_f = 15$ is plotted in Figure 3.17 by using the phasor tool in the EMTP-RV where *h* represents the order of the harmonics.

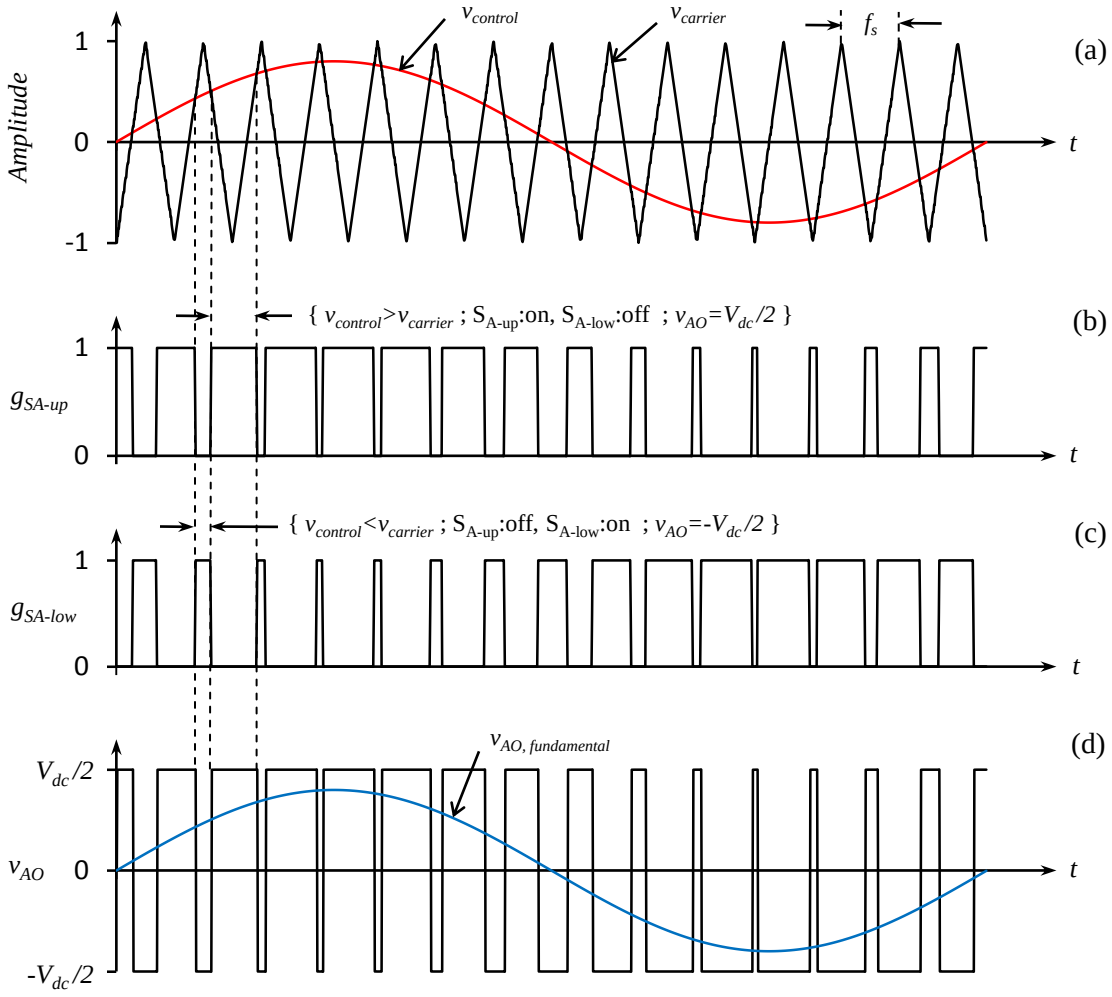


Figure 3.16: SPWM

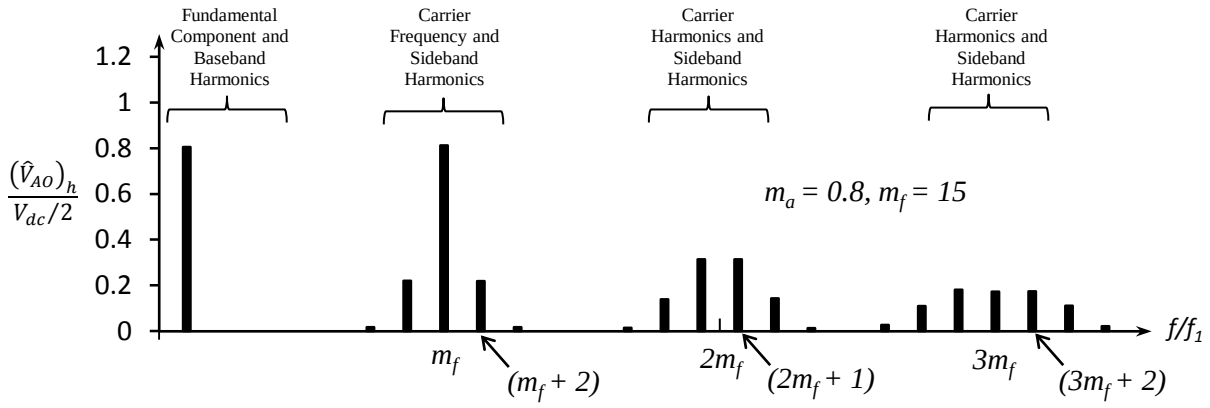


Figure 3.17: Harmonic amplitude spectrum.

When $m_a < 1.0$, the amplitude of the fundamental-frequency voltage varies linearly with m_a and the range of $0 < m_a < 1.0$ is called a "linear range" in SPWM. To increase further the amplitude of the fundamental-frequency component of the output voltage, m_a is increased beyond 1.0 resulting in what is so called *overmodulation*. Overmodulation causes the output voltage to contain more harmonics in baseband and sidebands as compared to the linear range, as shown in Figure 3.18. The harmonics with dominant amplitudes in the linear range may not be dominant during overmodulation. More significantly, with overmodulation, the amplitude of the fundamental-frequency component does not vary linearly with the amplitude modulation ratio m_a. Figure 3.19 shows the normalized peak amplitude of the fundamental-frequency component $\left(\hat{V}_{AO}\right)_1/\frac{1}{2}V_{dc}$ as a function of the amplitude modulation ratio m_a. $\left(\hat{V}_{AO}\right)_1/\frac{1}{2}V_{dc}$ depends on m_f in the overmodulation region at reasonably large value of m_f while it varies linearly with m_a, almost independent of m_f (provided $m_f > 9$) in the linear range ($m_a < 1.0$) [27].

The SPWM allows the control of the magnitude and the frequency of the output voltage. The input is uncontrolled, essentially a constant dc voltage source. This switching scheme gives harmonics in the range of the switching frequency and higher, which can be easily filtered out.

3.8.4 Multi-level concept

Multi-level converters have been receiving increased attention recently, especially for high-power high-voltage applications [28]. Increasing the number of voltage levels in the converter without requiring higher ratings on individual devices can increase the power rating.

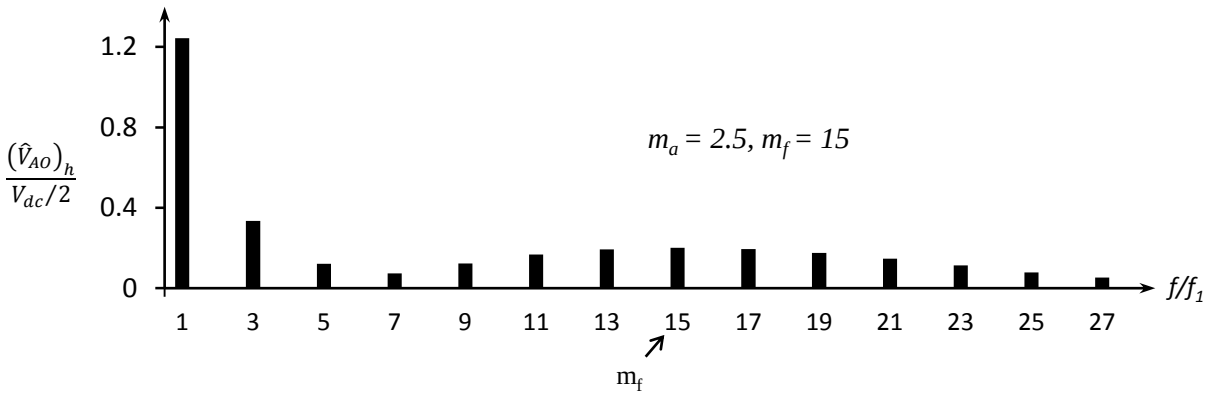


Figure 3.18: Harmonics due to overmodulation, $m_a = 2.5$ and $m_f = 15$.

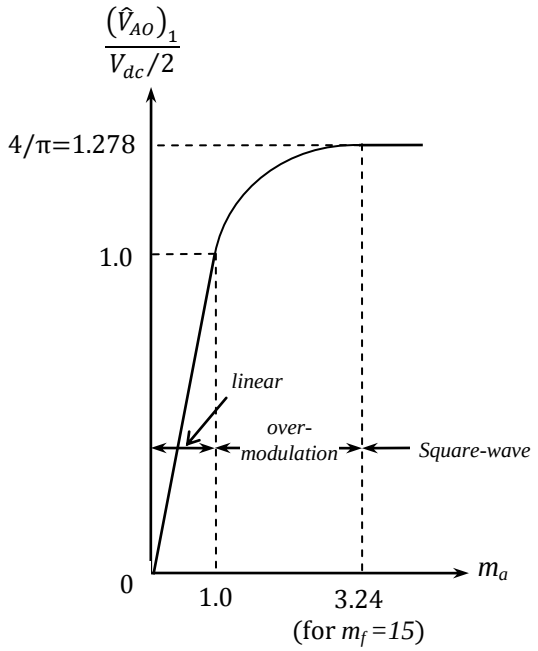


Figure 3.19: Voltage control by varying m_a.

The structure of multi-level voltage source converters allows them to reach high voltages with low harmonics without the use of series-connected switching devices. As the number of voltage levels increase, the harmonic content of the output voltage waveform decreases significantly [26].

Figure 3.20 shows a conceptual schematic for a one leg of a five-level converter. For generalization, it can be regarded as an m-level converter with (*m-1*) capacitors to obtain voltage levels of *m* number. The series-connected capacitors divide the V_{dc} into equal portions and

provide the nodes to which the switch can be connected which results in output voltage in different voltage levels. The output voltage v_{AO} is the voltage between nodes A and "O", the latter is the neutral point where zero voltage is obtained at the middle position (position 3) of the switch. Figure 3.21 illustrates the available voltage levels which can be obtained by connecting the switch in Figure 3.20 to one node at a time. The actual realization of the switch requires bidirectional switching devices for each node.

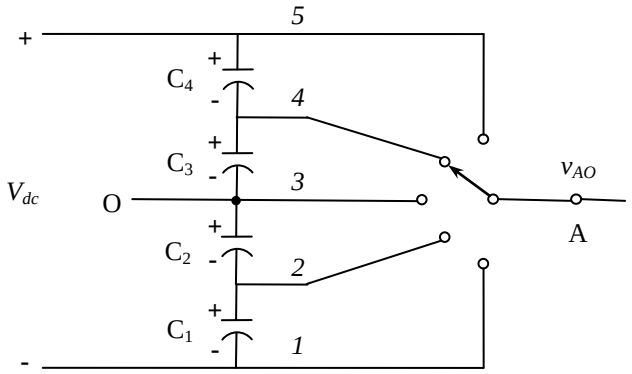


Figure 3.20: Schematic diagram of one leg of a multi-level converter by a switch.

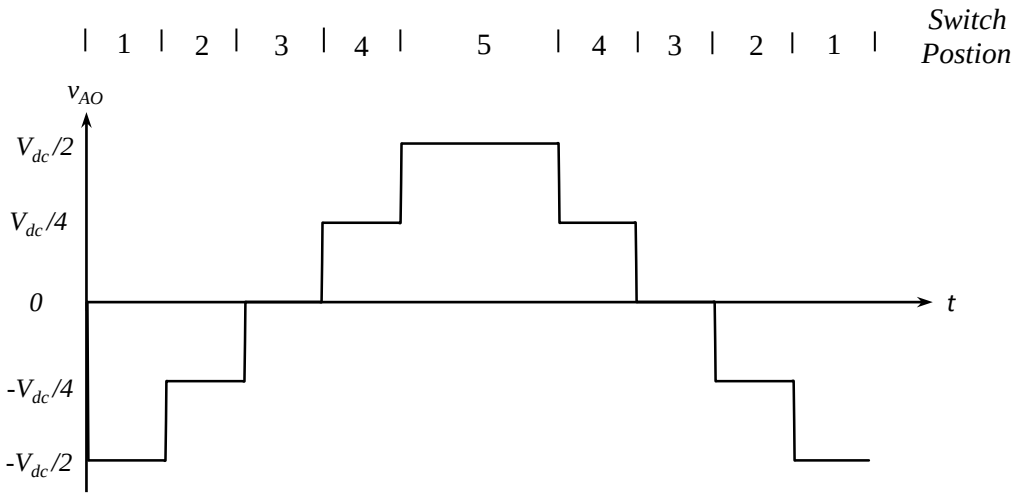


Figure 3.21: Waveform of v_{AO} in Figure 3.20.

3.9 Single-Phase Three-Level SPWM Converter

A single-phase three-level SPWM converter consists of two legs and two dc capacitors. Each leg has four bidirectional valves i.e. a power electronic circuit element with turn-on and

turn-off capability and an anti-parallel diode combination and two clamping diodes. This structure is very suitable for high power applications as it produces less harmonics, has smaller dc capacitors, lower switch blocking voltage and lower switching losses when compared to the two-level topology [29].

3.9.1 Circuit configuration

Figure 3.22 illustrates the power electronic circuit configuration of a single-phase three-level diode-clamped SPWM converter. IGBTs are used here as the switching elements with turn-on and turn-off capability. This arrangement receives gate patterns for the switching scheme from the gate pattern generator. This design enables the converter to switch not only between the upper and lower dc voltage levels but also allows the output to be zero voltage level as well. Hence, it is possible that each leg's output voltage can be in three different voltage levels with respect to the midpoint "O" (v_{AO} and v_{BO}).

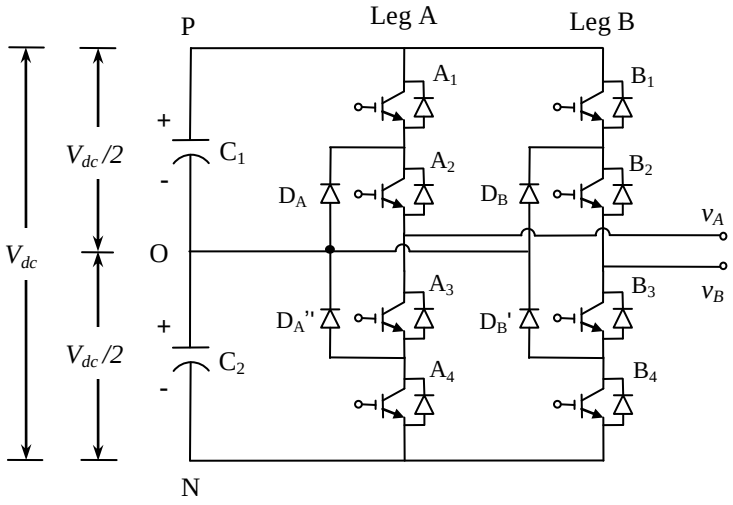


Figure 3.22: Single-phase three-level SPWM converter.

Figure 3.23 illustrates the change of output voltage in one leg where the switch and the clamping diode states can be seen in three different voltage levels at the output point with respect to node O in the inverter mode of operation. Figure 3.23(a) shows that when the upper two switches S_1, S_2 are on, the upper clamping diode D blocks the negative terminal of the upper dc capacitor to reach the middle point of the upper part of the leg which results in that the positive dc rail appears at the output point. Similarly, Figure 3.23(c) shows that when the lower two

switches S_3, S_4 are on, the lower clamping diode D' clamps the positive terminal of the lower capacitor, which results in the negative dc rail at the output point. In case of the zero voltage level, only one of the S_2-D and S_3-D' pairs is on, according to the polarity at the output terminal of the other leg. If the polarity is positive at the output terminal of the other leg, the S_3-D' pair is on. If the polarity is negative at the output terminal of the other leg, the S_2-D pair is on. Figure 3.23(b) illustrates these conditions in a generalized way.

Figure 3.24 shows that the voltage changes between zero and $+V_{dc}/2$ or between zero and $-V_{dc}/2$ voltage levels in every half-cycle for a leg. For this reason, this type of SPWM scheme is called a SPWM with a unipolar voltage switching, as opposed to the SPWM with bipolar (between $+V_{dc}$ and $-V_{dc}$) voltage switching scheme described in Section 3.8.2. This scheme has the advantage over the bipolar voltage switching scheme in terms of generating less harmonic levels as it is explained in Section 3.9.2.

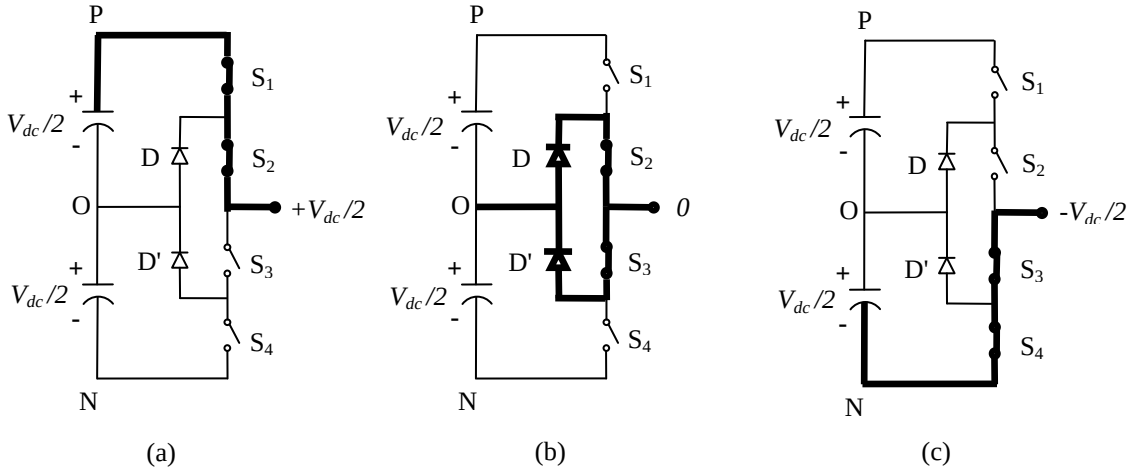


Figure 3.23: Change of the output voltage in one leg.

The switching scheme can be achieved by comparing $v_{control}$ and $-v_{control}$ with the carrier signals which are 180° out of phase. Figure 3.24 shows the carrier waves, the control waves, the output voltage of leg A and B with respect to point O, v_{AO} and v_{BO}, and the voltage between the output terminals A and B, v_{AB}. As it can be seen from Figure 3.24(e), this scheme enables an effective doubling of the switching frequency compared to the two-level classical SPWM scheme (Figure 3.16) resulting in a significantly lower harmonic content.

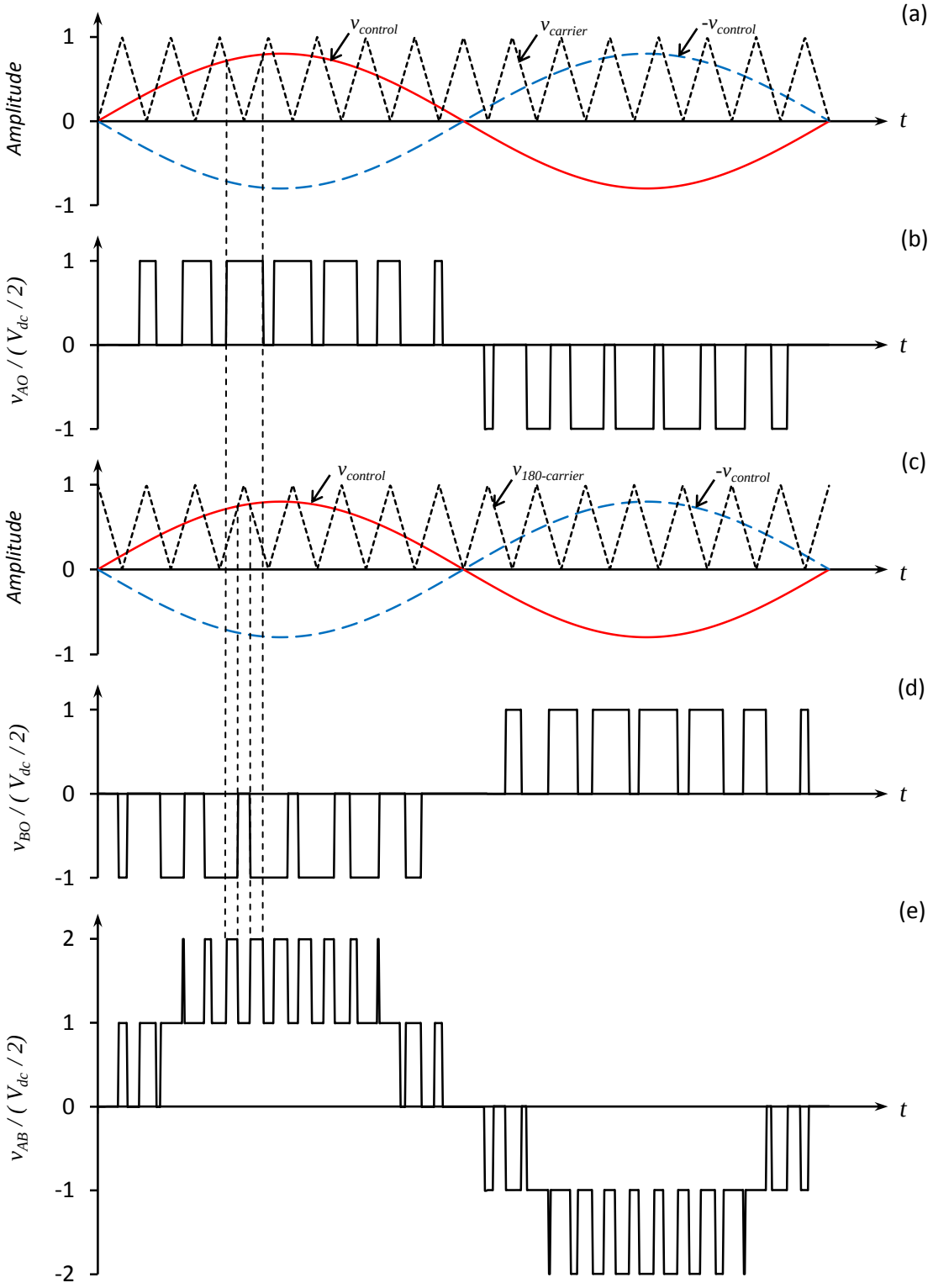


Figure 3.24: Output waveforms of a three-level unipolar SPWM converter (m_a= *0.8* and m_f=15).

3.9.2 Single-phase three-level SPWM switching

The SPWM gate pattern generator produces four gate signals, one for each IGBT in a given leg. The generation of the four gating signals is achieved by using two control signals and one unipolar triangular waveform carrier signal. A unipolar triangular waveform can be easily formed by using the same principle of the built-in PWM generator (triangular) in the library of the EMTP-RV (Version 2.2.1) in which the traditional bipolar triangular waveform is produced. The sequence of forming such a waveform, shown in Figure 3.25 is as follows:

1. A bipolar square-wave pulse train is generated from a signal generator at a specified amplitude and frequency. Here, the amplitude is 1.0 and the frequency is the switching frequency, f_s.
2. The square-wave signal is processed by an integral block to obtain a triangular waveform.
3. The amplitude of the triangle waveform signal is modified to the desired value.

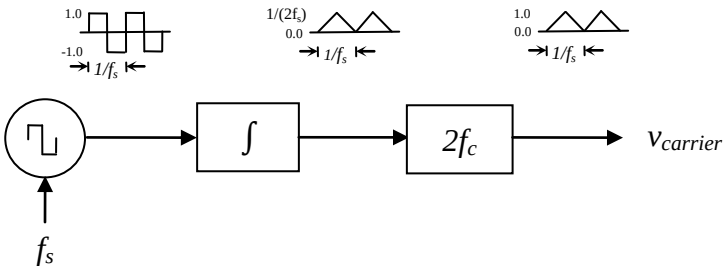


Figure 3.25: Generation of a unipolar triangular waveform carrier signal.

The state combinations for the four switches on one leg in Figure 3.23 and the resulting output voltages are given Table 3.1. Two comparators are used to generate the four switching signals required for one leg. The corresponding schematic diagram for the switching strategy for both legs is shown in Figure 3.26.

Table 3.1: Switching pattern for one leg of a single-phase three-level SPWM converter.

Switches				Output Voltage
S_1	S_2	S_3	S_4	
ON	ON	OFF	OFF	$+V_{dc} / 2$
OFF	ON	ON	OFF	0
OFF	OFF	ON	ON	$-V_{dc} / 2$

The comparison logic that matches Table 3.1 switching scheme for leg A is as follows:

Two control signals $v_{control}$ and $-v_{control}$ are compared with the triangular carrier signal $v_{carrier}$.

- If $v_{control} > v_{carrier}$, switch A_1 is ON, else switch A_1 is OFF.
- If $-v_{control} > v_{carrier}$, switch A_4 is ON, else switch A_4 is OFF.
- To avoid simultaneous connection to node O, only two switches can be turned ON at the same time. Thus, switches A_1 & A_3 and A_2 & A_4 are complementary.

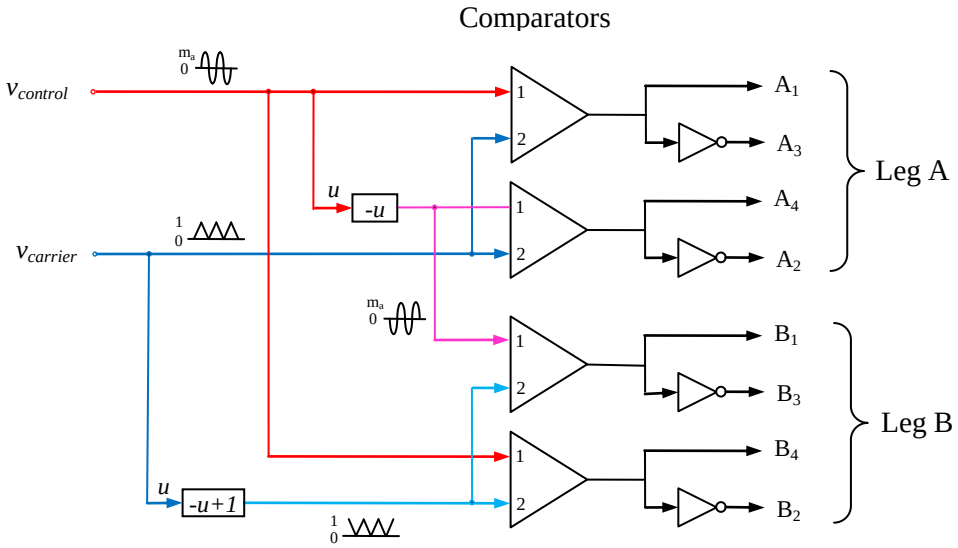


Figure 3.26: Schematic diagram of switching logic for single-phase three-level SPWM converter (*u* is the input signal for the corresponding block, not the global signal).

For leg B, the firing signals are produced by comparing the same two control signals $v_{control}$ and $-v_{control}$ with the triangular carrier signal shifted 180° in phase, $v_{180\ carrrier}$. The unipolar 180° phase-shifted triangular signal can be obtained simply by multiplying the triangular signal for leg A by -1, and then adding +1. The comparison logic for leg B is as follows:

- If $-v_{control} > v_{180\ carrier}$, switch B_1 is ON, else switch B_1 is OFF.
- If $v_{control} > v_{180\ carrier}$, switch B_4 is ON, else switch B_4 is OFF.
- To avoid simultaneous connection to node O, only two switches can be turned ON at the same time. Thus, switches B_1 & B_3 and B_2 & B_4 are complementary.

In accordance with the above comparison logics, the control and carrier signals, the four gate signals, the output waveforms measured to node O for leg A (v_{AO}) and leg B (v_{BO}) are illustrated in Figures 3.27 and 3.28, respectively.

Figure 3.29 illustrates the harmonic amplitude spectrum for v_{AO} waveform in Figure 3.27. The comparison between this figure and Figure 3.17 shows that the harmonic amplitude spectrum of the unipolar waveform is better than that of the bipolar PWM technique despite the fact that the same magnitude of the fundamental component can be achieved.

The harmonic amplitude spectrum for v_{AB} waveform in Figure 3.24(e) can be seen in Figure 3.30 where the amplitude is scaled to V_{dc}. It is apparent that the harmonics at the carrier frequency and its sidebands are disappeared due to the so-called effective frequency doubling. It is accomplished without increasing the switching frequency. The harmonics, which are easily filtered out, at the other frequencies (second, fourth harmonics of the carrier frequency etc. and their sidebands) are the same as those of v_{AO} in Figure 3.29.

3.10 SSSC Controller

The controller for the SSSC can be divided, generally, into two main controllers, namely internal and external controllers. The main function of the internal controller is to provide the control signal to drive the gate pattern generator of the power converter in order to generate a fundamental output voltage waveform with the desired magnitude and phase angle in synchronism with the ac power system. The function of the external controller, if exists, is to modify the reference signals which determine the functional operation of the SSSC in order to achieve the desired system performance. The block diagram of the SSSC controller is illustrated in Figure 3.31.

A measurement block is employed to obtain the necessary variables to be processed in the control process. The calculation of the injected reactance is achieved by dividing the injected voltage by the line current (rms values). The calculated injected reactance is then compared to the modified reference reactance (the sum of the reference reactance $X_{ref\text{-}pu}$ and the supplementary controller reactance X_{supp}) and the difference is fed to a PI controller (for magnitude control) for the control action. The output of the PI controller forms the modulation

index which determines the amplitude of the control signal. The modulation index is limited by a limiter to prevent overmodulation beyond a set upper limit.

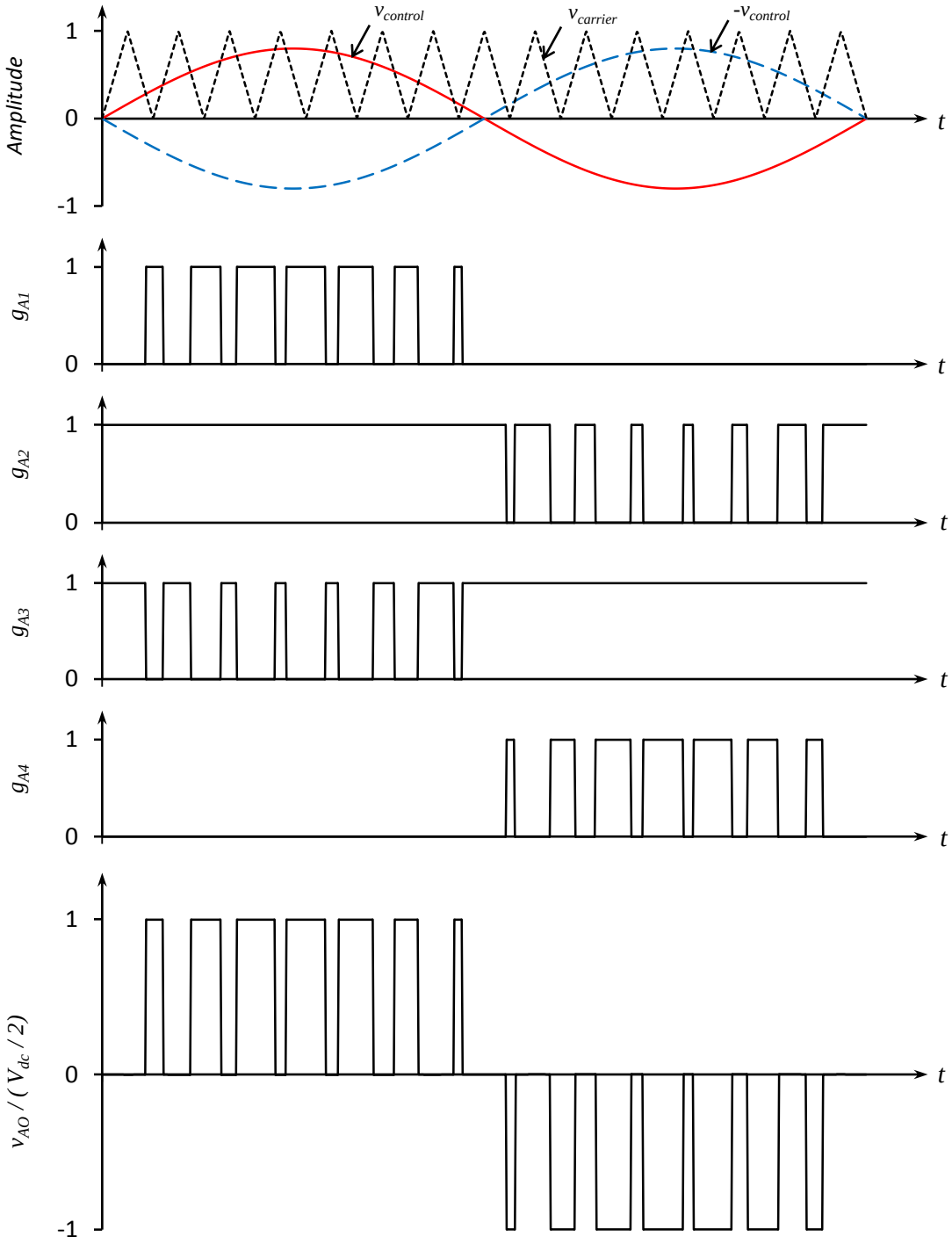


Figure 3.27: Three-level unipolar SPWM switching pulses and output voltage waveform v_{AO} for Leg A (m_a = *0.8* and m_f = 15).

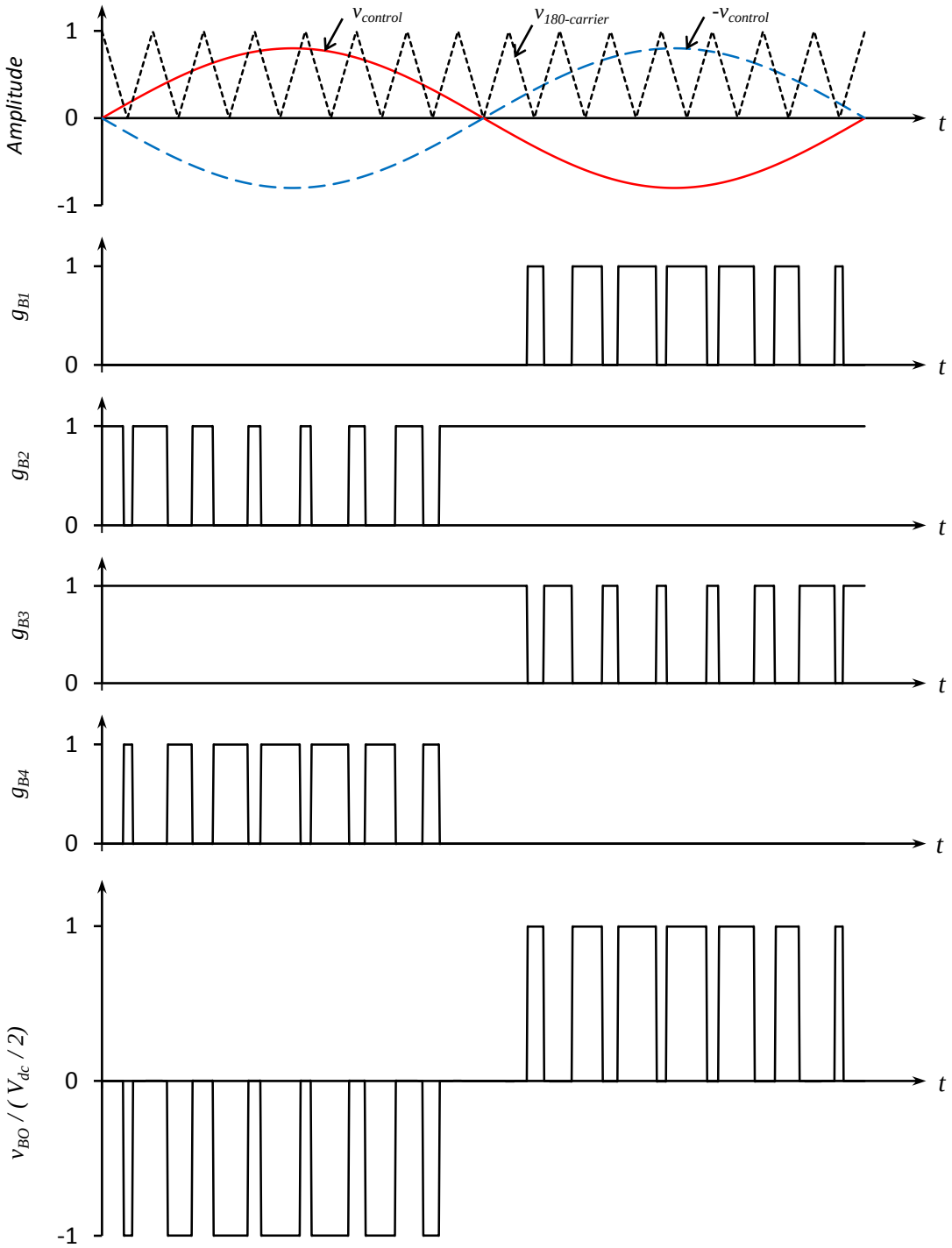


Figure 3.28: Three-level unipolar SPWM switching pulses and output voltage waveform v_{BO} for Leg B (m_a = *0.8* and m_f = 15).

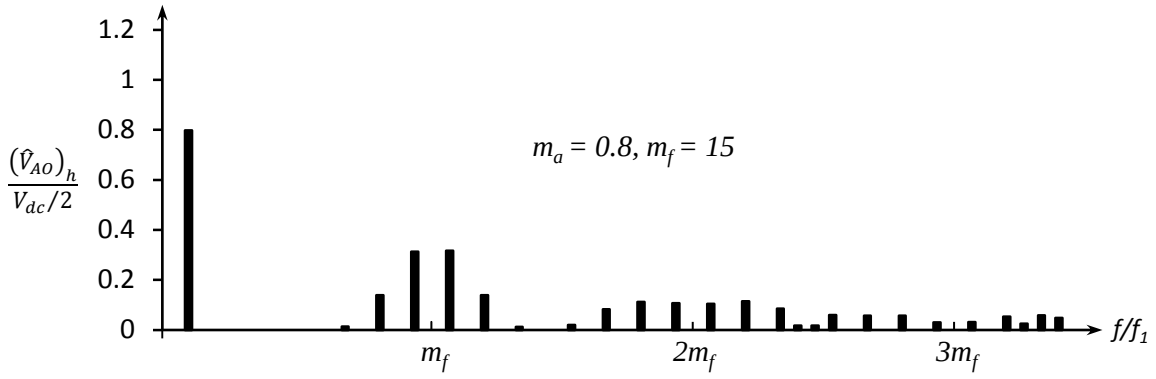


Figure 3.29: Harmonic amplitude spectrum for v_{AO}.

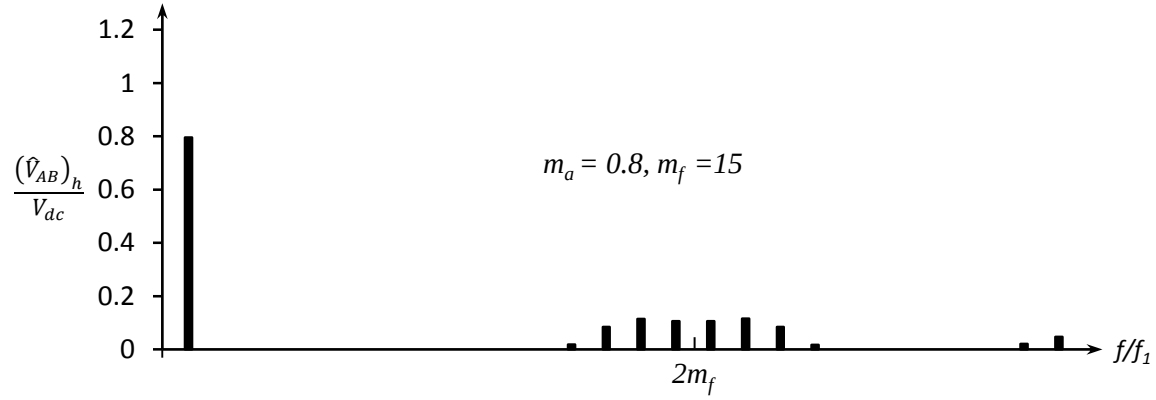


Figure 3.30: Harmonic amplitude spectrum for v_{AB}.

A phase-locked loop (PLL) is used to extract the phase angle of the line current which is necessary for synchronization with the power system (more discussion on this PLL is given in Subsection 3.10.2). A $\pm\pi/2$ is added to the system angle, Θ_{sys}, depending on the operating mode of the SSSC. If the SSSC is required to operate as an inductive compensator, $+\pi/2$ is added and the injected voltage leads the line current by 90°. If $-\pi/2$ is added, the injected voltage lags the line current by 90° and the SSSC is operating as a capacitive compensator.

A dc-side voltage controller is formed separately in order to maintain the dc capacitor voltage constant. In such a controller, the measured dc capacitor voltage is compared to the desired reference dc voltage and the difference is fed to a PI controller that generates a small angle displacement, $\Delta\Theta_{dc}$, which is added to the sum of Θ_{sys} and $\pm\pi/2$. This small angle

displacement locates the SSSC's steady-state operating point in the "absorb P – supply Q" quadrant in Figure 3.4(a). In other words, the SSSC draws a small amount of real power from the ac power system for replenishing its losses. The summation of the angles (Θ) as an argument is sent to a sine block that produces a sine waveform with amplitude of one and frequency of 60 Hz. This waveform is multiplied by the modulation index resulting in the control signal $v_{control}$. This control signal is fed to the gate pattern generator and compared to the triangular carrier signal.

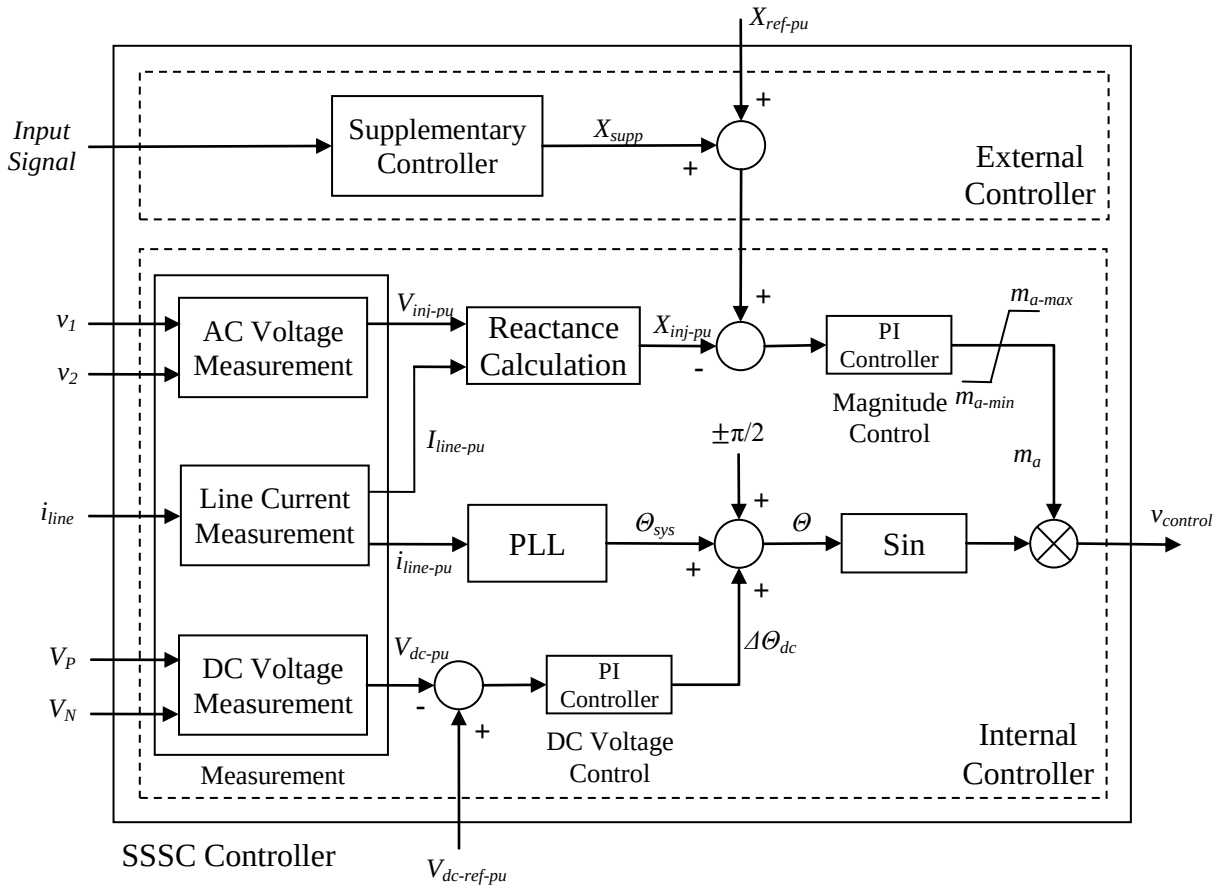
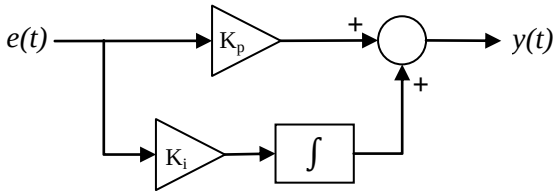


Figure 3.31: SSSC controller block diagram.

PI Controller: In many control problems, it is important to reduce the steady-state error to almost zero. For this purpose, a proportional-integral (PI) controller is useful [30]. It has the primary virtue that its output at the steady-state can be a nonzero constant value even when the error signal at its input is zero. This is because the integrator sums all past values of the input error signal. A maximum and a minimum limit can be inserted on the output path so that the

unwanted output values are prevented. Figure 3.32 shows a typical schematic of a PI controller. In the investigations conducted in this thesis, PI controllers are tuned-up by a trial-and-error technique through changing K_p and K_i in small increments.



$$y(t)=K_p e(t) + K_i \int e(t)dt$$

Figure 3.32: A PI controller.

3.10.1 Measurement block

In the measurement block of Figure 3.33, the received quantities at the inputs are processed to form the control variables which are used in the control processes. These received quantities are converted to per unit values as the controller is designed on per unit (p.u.) scale. The versatility of the p.u. controller is that it can be used for all kinds of voltage and current levels with small changes (or no change) to the designed operating condition control parameters. The p.u. ac quantities are filtered using bandpass filters to obtain the fundamental frequency component of the corresponding signals. These are sent to root-mean-square (RMS) blocks that calculate their rms values.

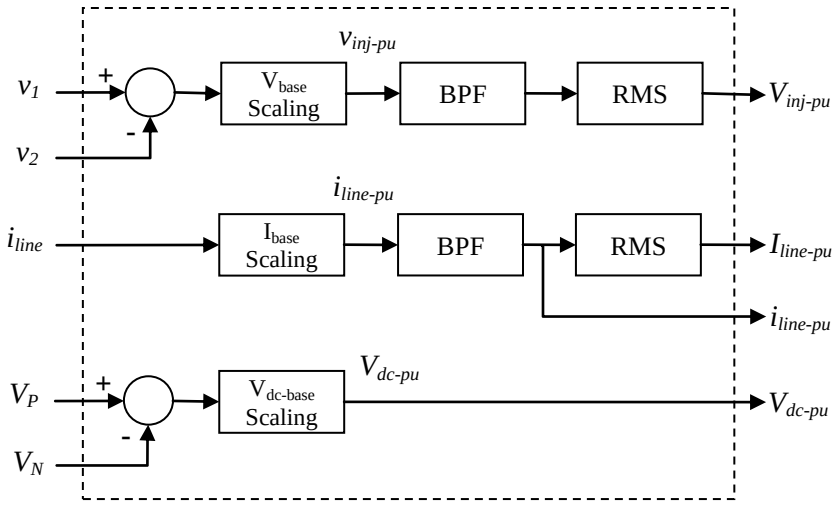


Figure 3.33: The measurement block.

Bandpass Filter: The transfer function and Bode plots of the second-order bandpass filter used in the measurement block of Figure 3.33 are shown in Figure 3.34. This filter which has a center frequency of 60 Hz (377 rad/sec) is designed using MATLAB.

$$T_{BP\ filter}(s) = \frac{188.5s + 1.071 \cdot 10^{-11}}{s^2 + 188.5s + 142120} \tag{3.11}$$

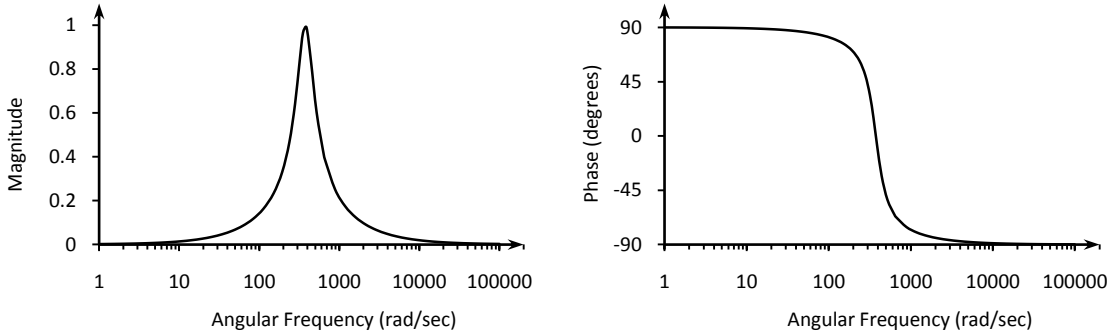


Figure 3.34: Bode plots of the bandpass filter: (a) magnitude response, (b) phase response.

3.10.2 Phase-locked loop (PLL)

To operate the SSSC in synchronism with the power system, the value of the instantaneous phase angle of the system is required. Phase-locked loops are widely used in several engineering applications to extract the phase and frequency information for signals. The main idea behind phase-locking is the ability to generate a sinusoidal signal whose phase is coherently following that of the main component of the input signal.

The PLL shown in Figure 3.35 consists of three building blocks; a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). The PD is conventionally a multiplier and the LF is a low-pass filter. The VCO generates an output signal such that its phase angle is in lock with that of the input signal [31].

A refined variant of the VCO signal is subtracted from the input signal that produces an intermediary error signal. This signal is then multiplied by the output of the VCO and is fed to the LF. The output of the VCO is θ_{sys} which is sent to the angle summation block of Figure 3.31.

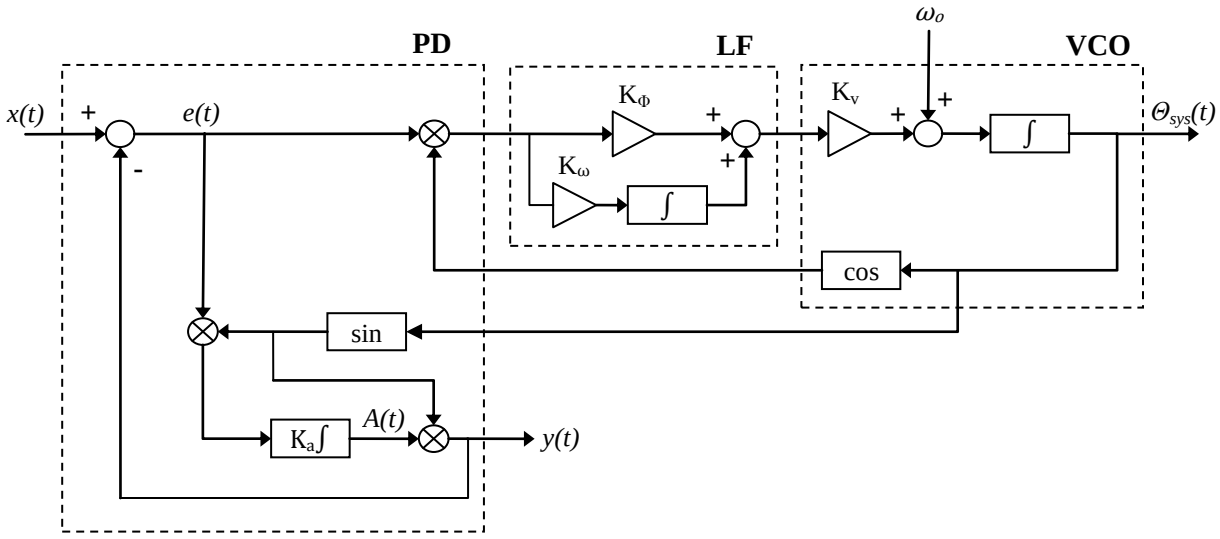


Figure 3.35: PLL schematic.

3.11 SSSC Implementation

A complete single-phase-SSSC as shown in Figure 3.36 is implemented in the EMTP-RV using the circuits and blocks described in Section 3.10. A step-up coupling transformer is used to interface the SSSC to the power system. It steps up the low voltage level at the converter output side to high voltage level at the transmission system side. A low-pass LC filter is used to filter out the harmonics.

Voltages and current are measured at the high voltage ac side. The differential voltage $v_{12} = v_1 - v_2$ is used to obtain the injected voltage, v_{inj} to the power system. The line current is used to obtain its phase angle for the aim of synchronism and to calculate the injected reactance of the SSSC, $X_{inj} = V_{inj} / I_{line}$. The parameters inside the controllers are tuned up based on trial-and-error as it is mentioned earlier. The electrical parameters of the SSSC shown in Figure 3.36 are presented in Table 3.2.

Table 3.2: Electrical parameters of the SSSC.

Coupling Transformer	
S = 100 MVA	V_2 / V_1 = 66 kV / 3.3 kV
X_{tr} = 0.1 p.u.	R_{tr} = 0.001 p.u.
LC Filter	L_f = 1 mH, C_f = 660 μF
Carrier Signal Frequency	f_s = 900 Hz

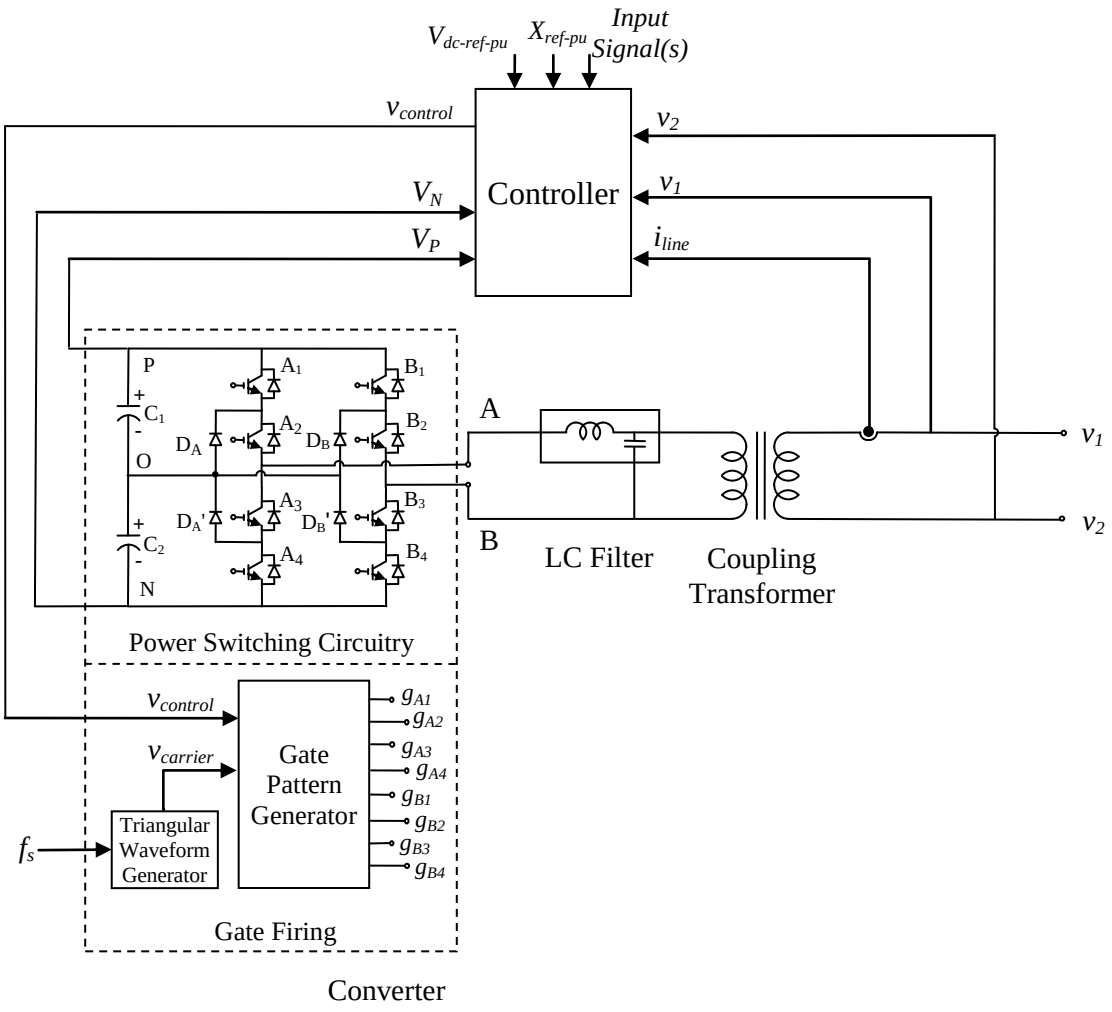


Figure 3.36: Single-phase-SSSC implementation.

3.12 Summary

This chapter has presented the concept of series capacitive compensation in the transmission system using capacitors and SSSC. The basic principles of the SSSC and SPWM are discussed. Moreover, the hybrid single-phase-SSSC compensation scheme and modeling of the single-phase-SSSC in the EMTP-RV are presented.

The effectiveness of the hybrid single-phase-SSSC compensation scheme in damping power system oscillations is investigated in the next chapter.

Chapter 4

DAMPING POWER SYSTEM OSCILLATIONS USING THE HYBRID SINGLE-PHASE-SSSC COMPENSATION SCHEME

4.1 General

The control offered by the SSSC is a 'source' type control, i.e. the inserted voltage is independent of the line current. This type of control normally is best suited to applications in power flow corridors, where a well-defined phase angle difference exists between the ends of the transmission line to be compensated and controlled. An SSSC can also be used, however, to provide additional damping to the electromechanical (0.5 - 2 Hz) power oscillations as it provides fast speed of response and executes any switching patterns without such restrictions that might apply for mechanical breakers.

In this chapter, the effectiveness of the hybrid single-phase-SSSC compensation scheme in damping power system oscillations is investigated. For this purpose, the scheme is assumed to be installed in one or more circuits of lines L_1 and L_2 replacing the fixed series capacitor compensations as well as in the uncompensated line L_3. The performance of the scheme in each case study is compared to the corresponding case with only fixed capacitor compensation.

4.2 SSSC Power Oscillations Damping Controller

The SSSC can be made to vary the series-compensation level dynamically in response to the controller-input signal so that the resulting changes in the power flow enhance the system damping. The traditional type of controller for Power Oscillations Damping (POD) purposes uses cascade-connected washout filters and linear lead-lag compensators to generate the desired reactance modulation signal. The purpose of the wash-out filters is to eliminate the average and extract the oscillating part of the input signal. The lead-lag compensators provide the desired phase shift at the oscillation frequency. Such a controller is illustrated in Figure 4.1 [32], [33], [34]. In some situations, a simple controller consists of only the washout filters can have a better

performance than that of the lead-lag controller. Such a controller, shown in Figure 4.2 can be regarded as a proportional type controller.

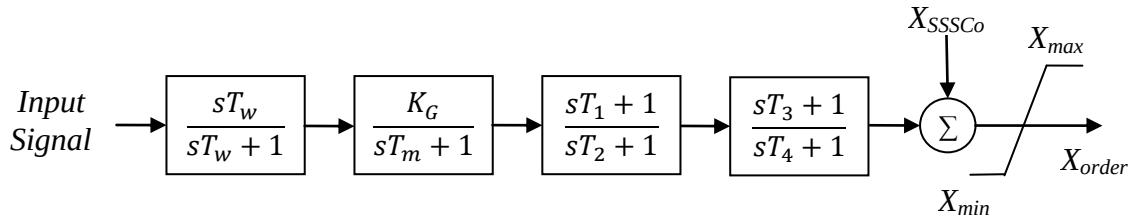


Figure 4.1: Structure of a lead-lag POD controller.

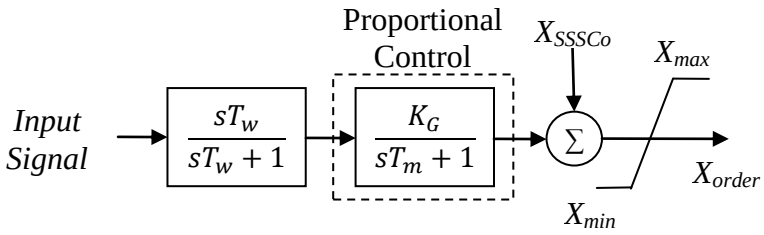


Figure 4.2: Structure of a simple POD controller.

The selection of the appropriate input (stabilizing) signal is an important issue in the design of an effective and robust controller. The selected input signal must yield correct control action when a severe fault occurs in the system. As an example, it was reported in [35] that if the real power is used as the input signal of a pure derivative controller, the output control signal may cause negative damping effects in the presence of disturbances involving large changes in the generator power angles.

The input signals could be local (e.g. real power flows) or remote (e.g. load angles or speed deviations of remote generators). If a wide-area network of Synchronized Phasor Measurement (SPM) units is available, then the remote signals can be downloaded at the controller in real time without delay [36] - [40]. In the studies conducted in this thesis, the generator load angles and speeds, measured with respect to the load angle and speed of a reference generator, as well as the real power flows in lines L_1 and L_2 are used as input signals.

It is worth noting here that due to the inherent imbalance nature of the hybrid single-phase-SSSC compensation scheme during transients, the design of the SSSC supplemental controller using classical linear control techniques would be very difficult, if not, virtually impossible to achieve. However, nonlinear control theories for FACTS applications have been

found to have a significant potential in recent years [41]. Some of the examples are; variable-structure controllers, model reference adaptive controllers and self-tuning controllers. Variable-structure controllers are capable of maintaining a desired response characteristic almost independent of the system structure. The design of any of such controllers is, however, beyond the level of being a part of a Master research project. In the studies conducted in this thesis, the supplemental controller parameters are determined by performing multiple time domain simulations with the aim of improving the transient responses of the system. In the case of multiple controllers, simultaneous tuning of the parameters of the controllers is performed to ensure that satisfactory dynamic and steady-state performances are met whilst minimizing or preventing undesirable interactions among controllers.

4.3 Case Study I: The Hybrid Single-Phase-SSSC Compensation Scheme is Installed in one Circuit of Line L_1

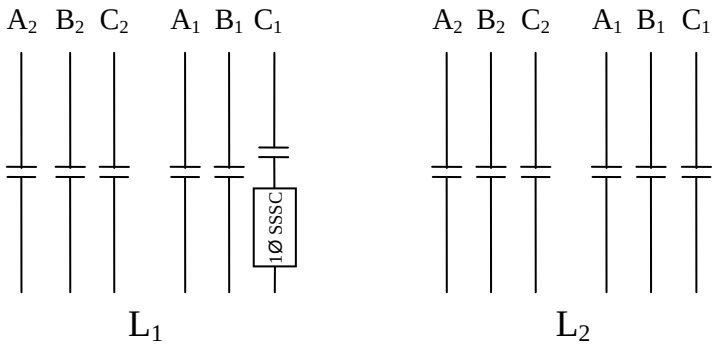


Figure 4.3: Case Study I: The hybrid single-phase-SSSC compensation scheme is installed in one circuit of line L_1.

The SSSC provides 50% of the total capacitive compensation ($X_{Cc} = X_{SSSC} = 0.5\ X_C$, Fig. 3.5) and the stabilizing signal is δ_{21}. The generator load angles and speeds, measured with respect to generator 1 load angle and speed, and the transmission line real power flow responses during and after clearing a three-cycle, three-phase fault at bus 4 are illustrated in Figures 4.4 to 4.6 for the case when the SSSC supplemental controller is of a proportional type with a transfer function given by Equation 4.1. Figures 4.7 to 4.9 illustrate the responses of the same variables

in the case when the SSSC supplemental controller is of a lead-lag type with a transfer function given by Equation 4.2.

$$G_P(s) = 0.75\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{4.1}$$

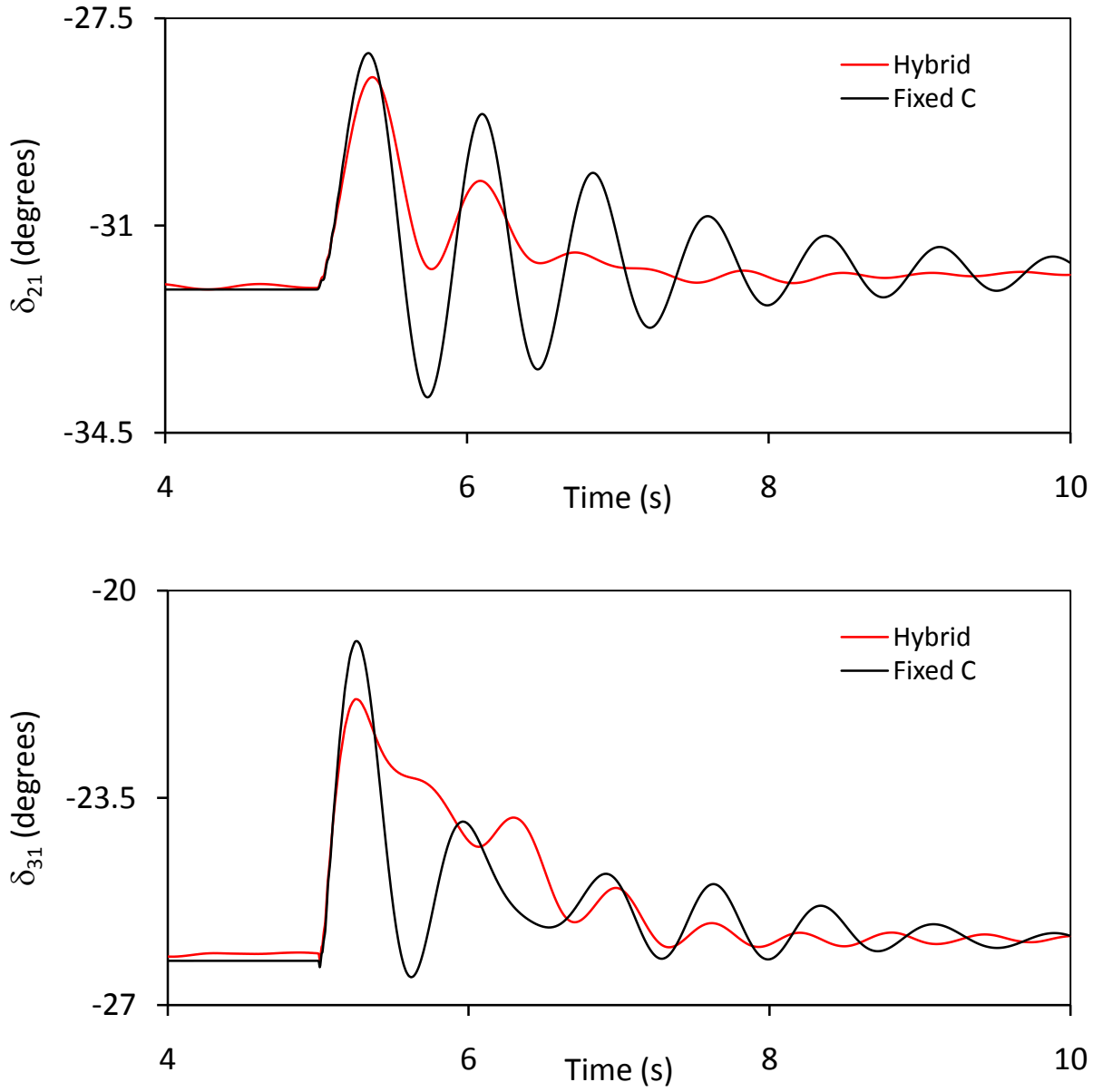


Figure 4.4: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I, SSSC supplemental controller: proportional type).

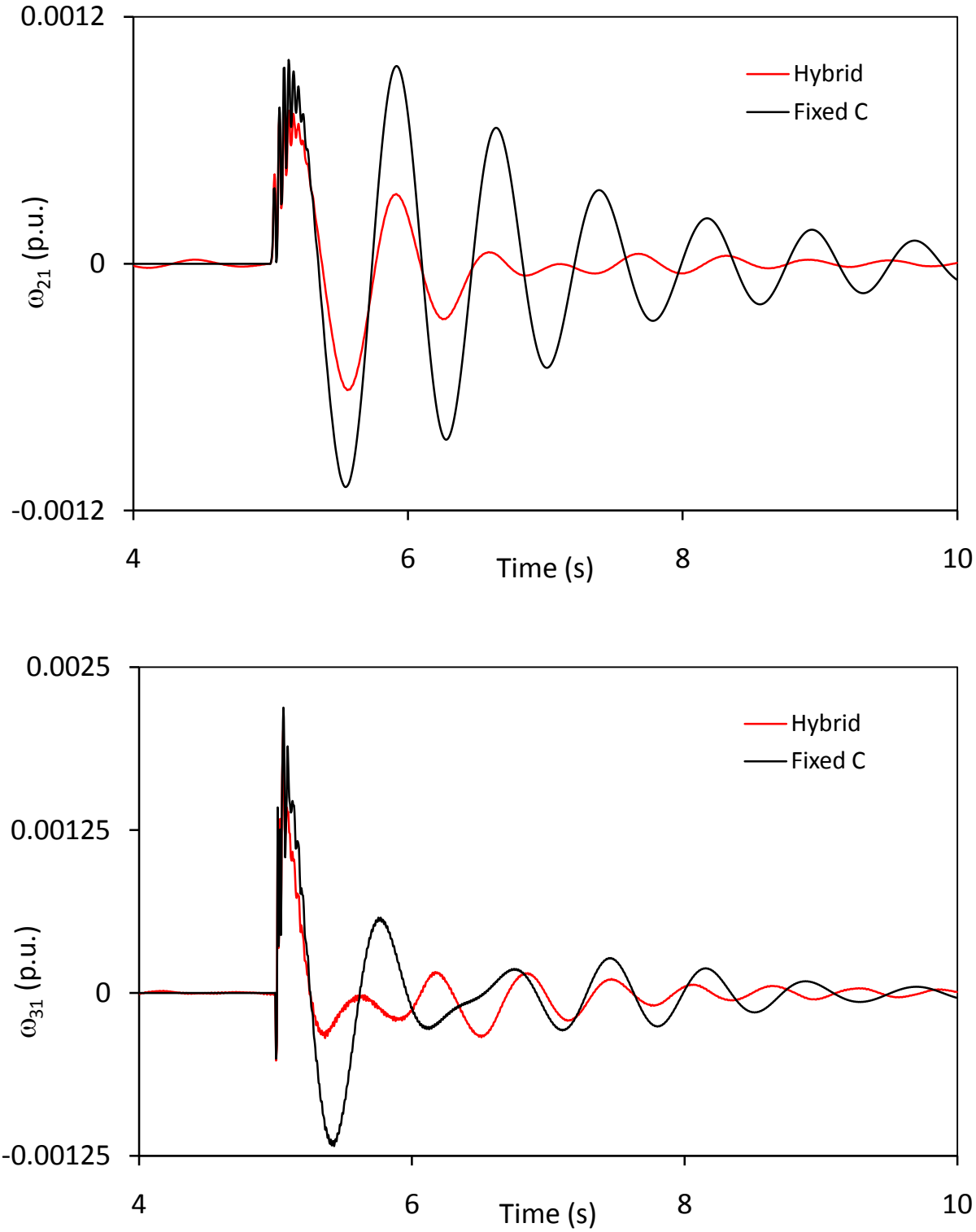


Figure 4.5: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I, SSSC supplemental controller: proportional type).

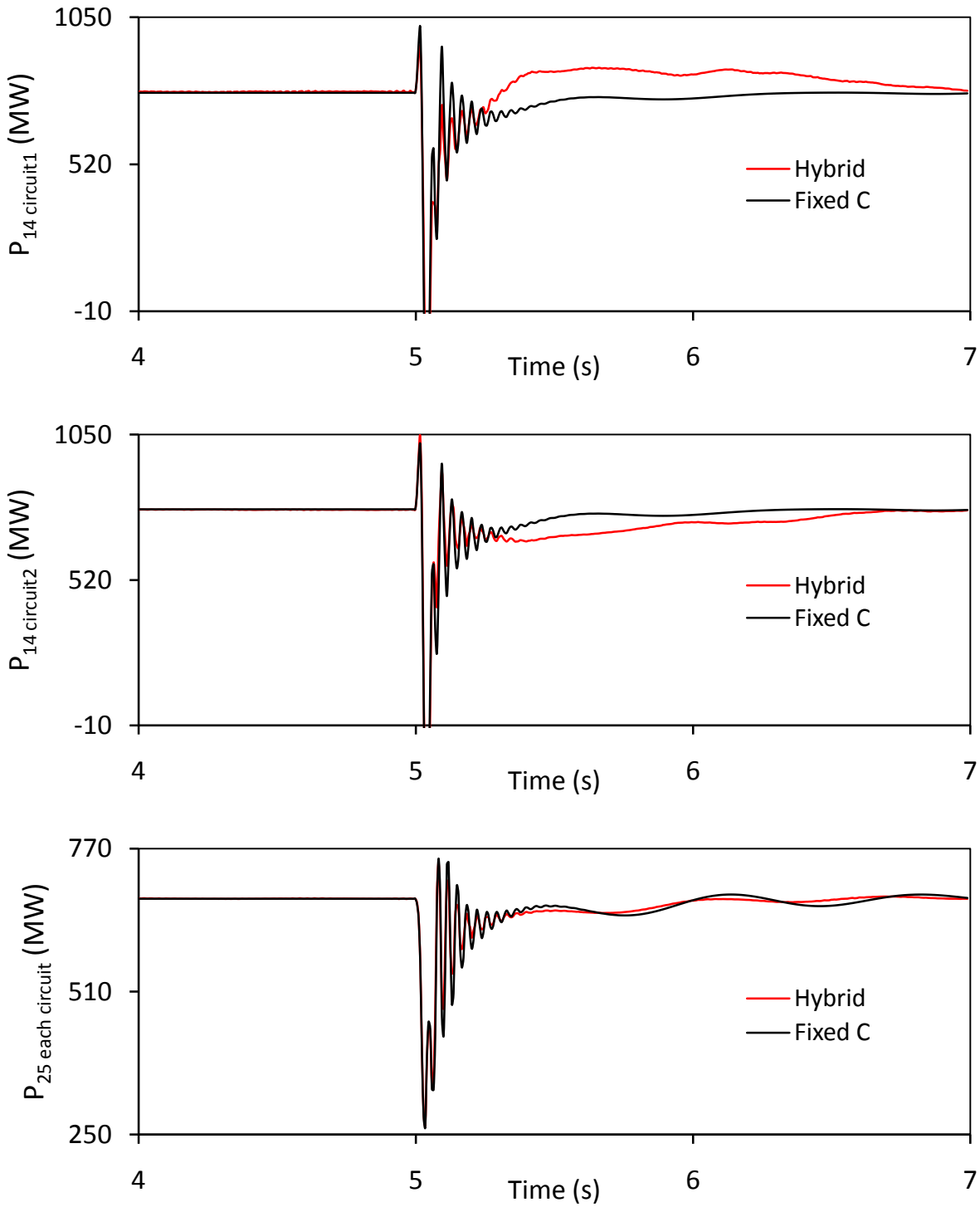


Figure 4.6: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I, SSSC supplemental controller: proportional type).

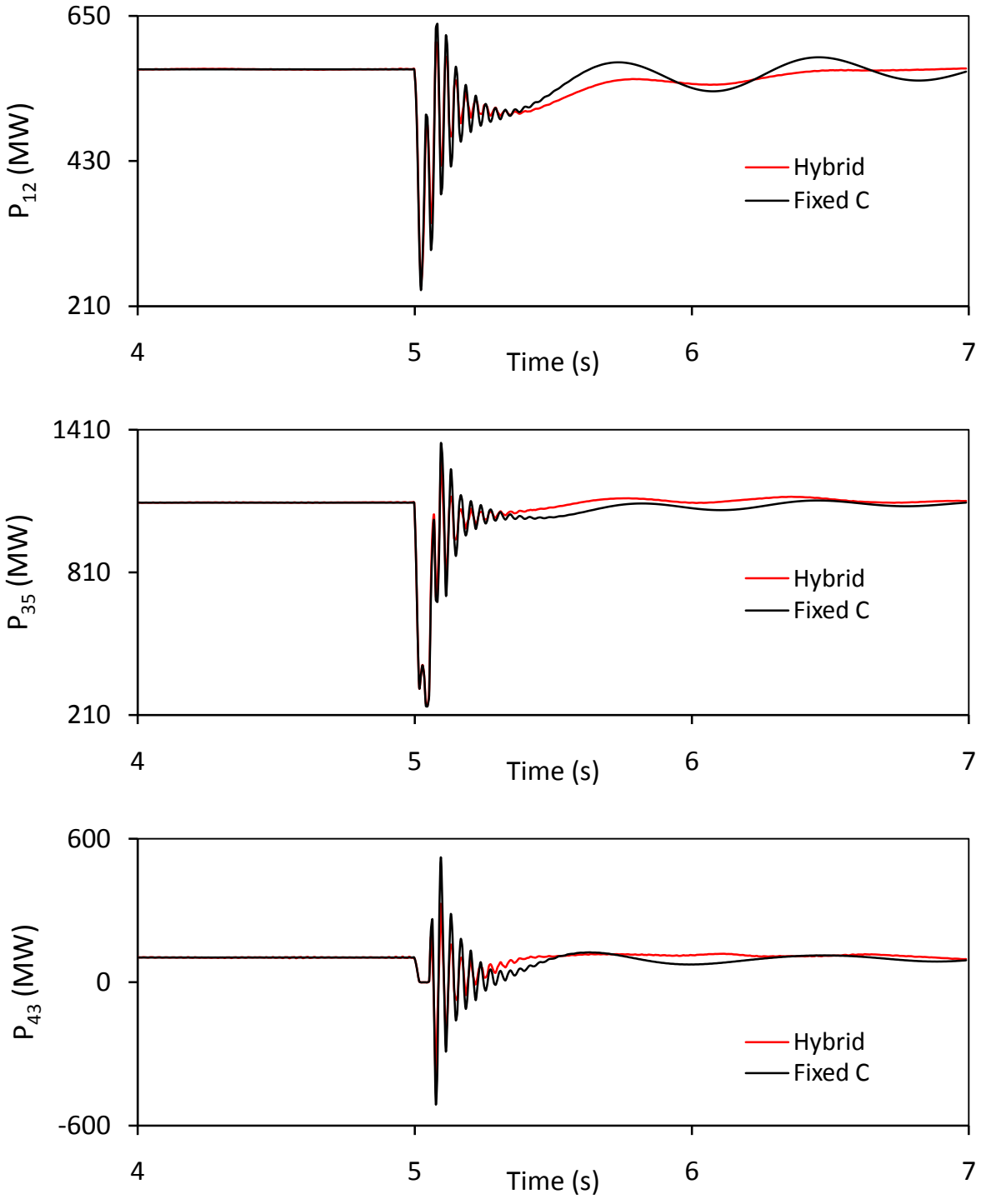


Figure 4.6: continued.

$$G_{L-L}(s) = 0.5\frac{15}{(s+15)}\frac{2s}{(2s+1)}\frac{(0.1097s+1)}{(0.1306s+1)}\frac{(0.1097s+1)}{(0.1306s+1)} \tag{4.2}$$

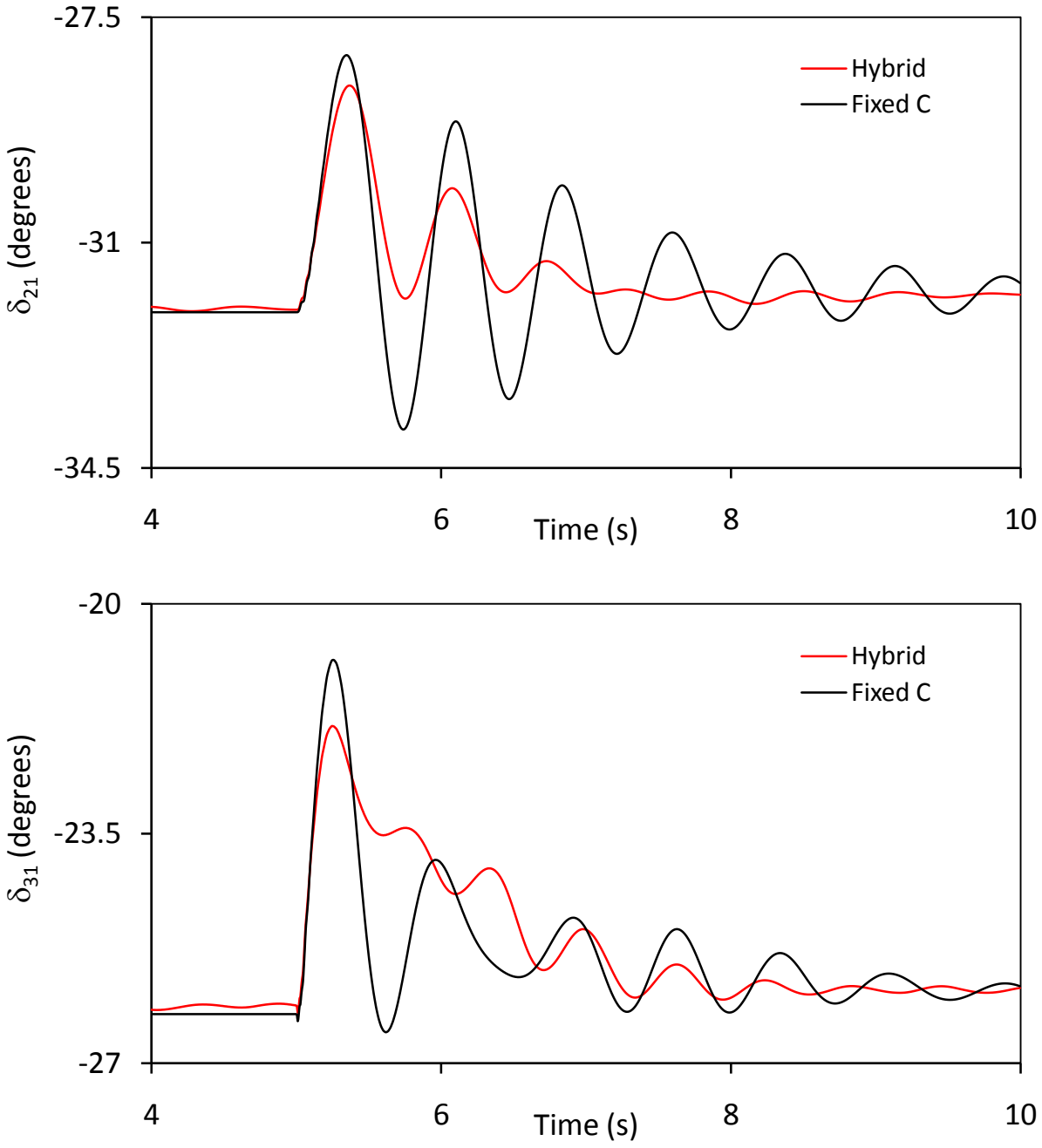


Figure 4.7: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I, SSSC supplemental controller: lead-lag type).

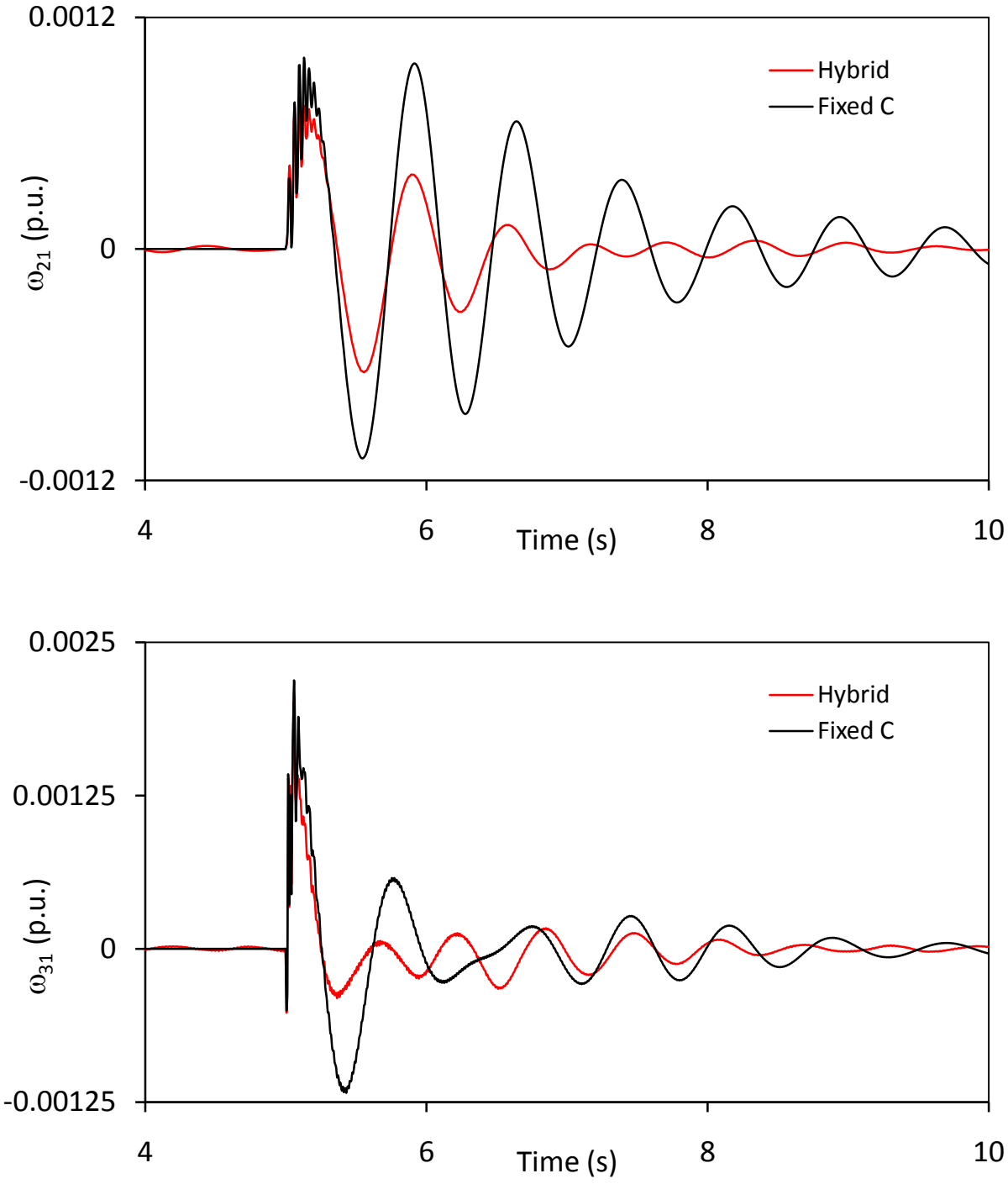


Figure 4.8: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I, SSSC supplemental controller: lead-lag type).

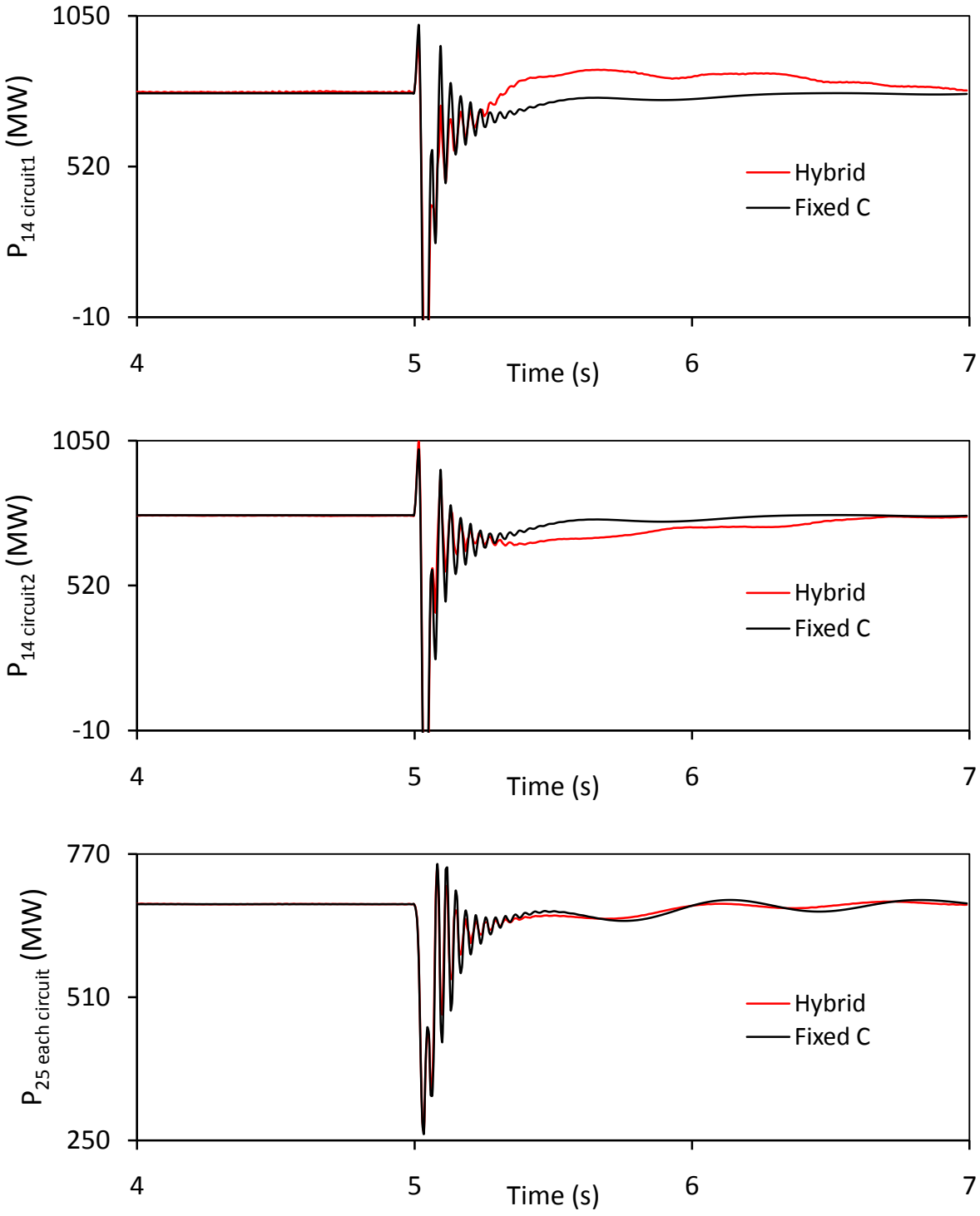


Figure 4.9: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I, SSSC supplemental controller: lead-lag type).

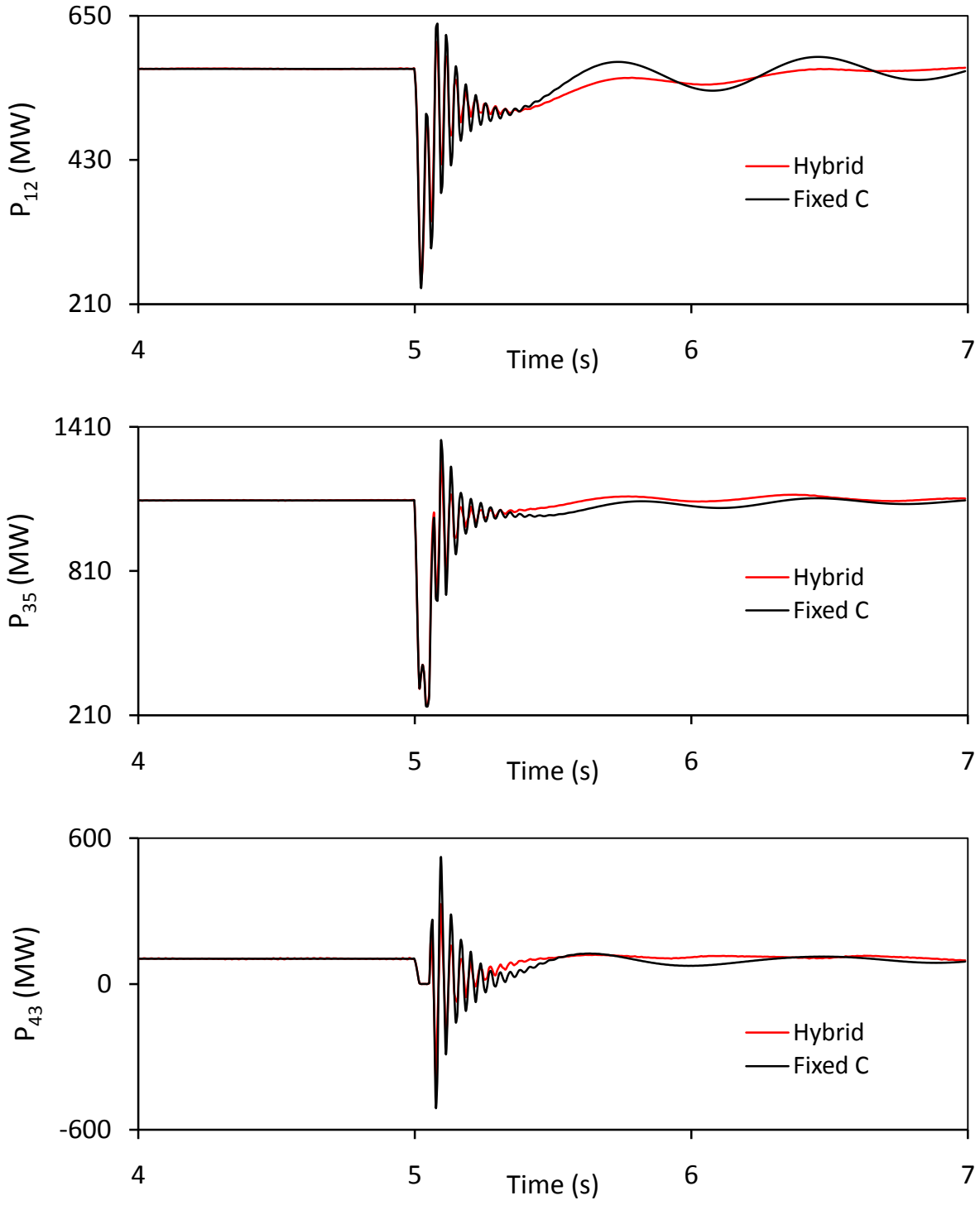


Figure 4.9: continued.

It can be seen from Figure 4.4 that in the case of fixed capacitor compensation, the system is first swing stable for this fault, but the post-contingency oscillations are not well damped. It can also be seen from Figures 4.4 and 4.7 that the effect of the SSSC supplemental controllers on the first swing is insignificant. The same figures show, however, that the SSSC supplemental controllers reduces the subsequent swings and provide a better damping than in the case of fixed capacitor compensation. Regarding the real line power flows, Figures 4.6 and 4.9 show that in the case of the hybrid single-phase-SSSC scheme, high spikes occur during the fault period.

The comparison between the performance of the proportional and the lead-lag controllers of Equations 4.1 and 4.2 is shown in Figure 4.10. It can be seen from this figure that the proportional controller results in a relatively better system transient response in terms of the settling time.

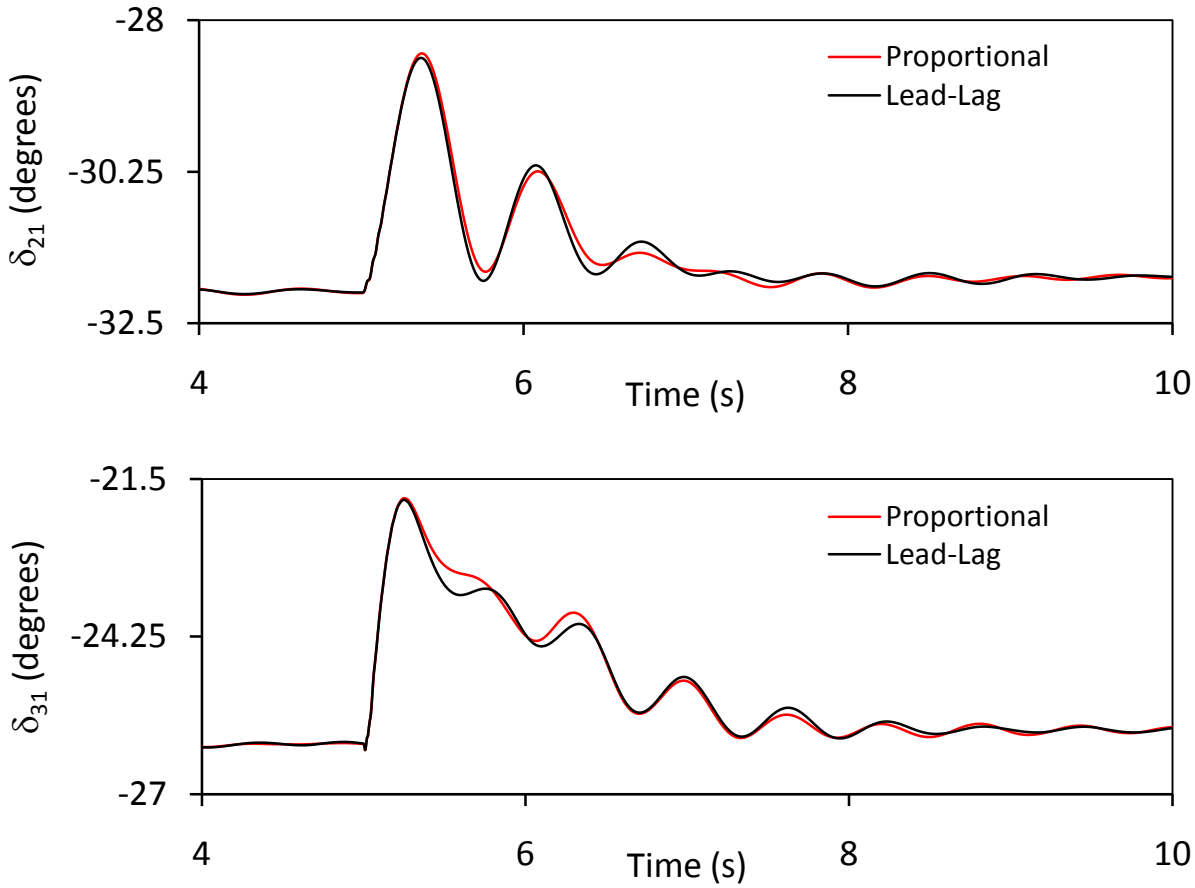


Figure 4.10: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study I).

4.4 Case Study II: The Hybrid Single-Phase-SSSC Compensation Scheme is Installed in one Circuit of Line L_2

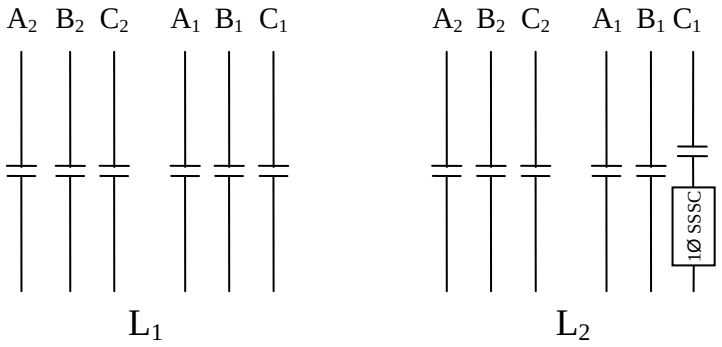


Figure 4.11: Case Study II: The hybrid single-phase-SSSC compensation scheme is installed in one circuit of Line L_2.

The SSSC provides 50% of the total capacitive compensation and the stabilizing signal is δ_{21}. The generator load angles and speeds, measured with respect to generator 1 load angle and speed, and the transmission line real power flow responses during and after clearing a three-cycle, three-phase fault at bus 5 are illustrated in Figures 4.12 to 4.14 for the case when the SSSC supplemental controller is of a proportional type with a transfer function given by Equation 4.3. The comparison between Figures 4.12 to 4.14 and Figures 4.7 to 4.9 shows that the system responses in Case Study I is better than those in Case Study II.

$$G_P(s) = -0.2\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{4.3}$$

Figures 4.15 to 4.17 illustrate the generator load angles and speeds, measured with respect to generator 1 load angle and speed, and the transmission line real power flow responses during and after clearing a three-cycle, three-phase fault at bus 2. This is a severe disturbance as the fault is at the terminals of a generating station. Time domain simulation results (not documented in this thesis) have shown that with a proportional controller and 50% of the total capacitive compensation provided by the SSSC, satisfactory system damping is not achievable. When the SSSC is set to provide the total degree of compensation (i.e. $X_{Cc} = 0$), Figures 4.15 to 4.17 show that a slight improvement in the system damping is obtained that the SSSC

supplemental controller with a transfer function is given by Equation 4.4 and the stabilizing signal is δ_{21}.

$$G_P(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{4.4}$$

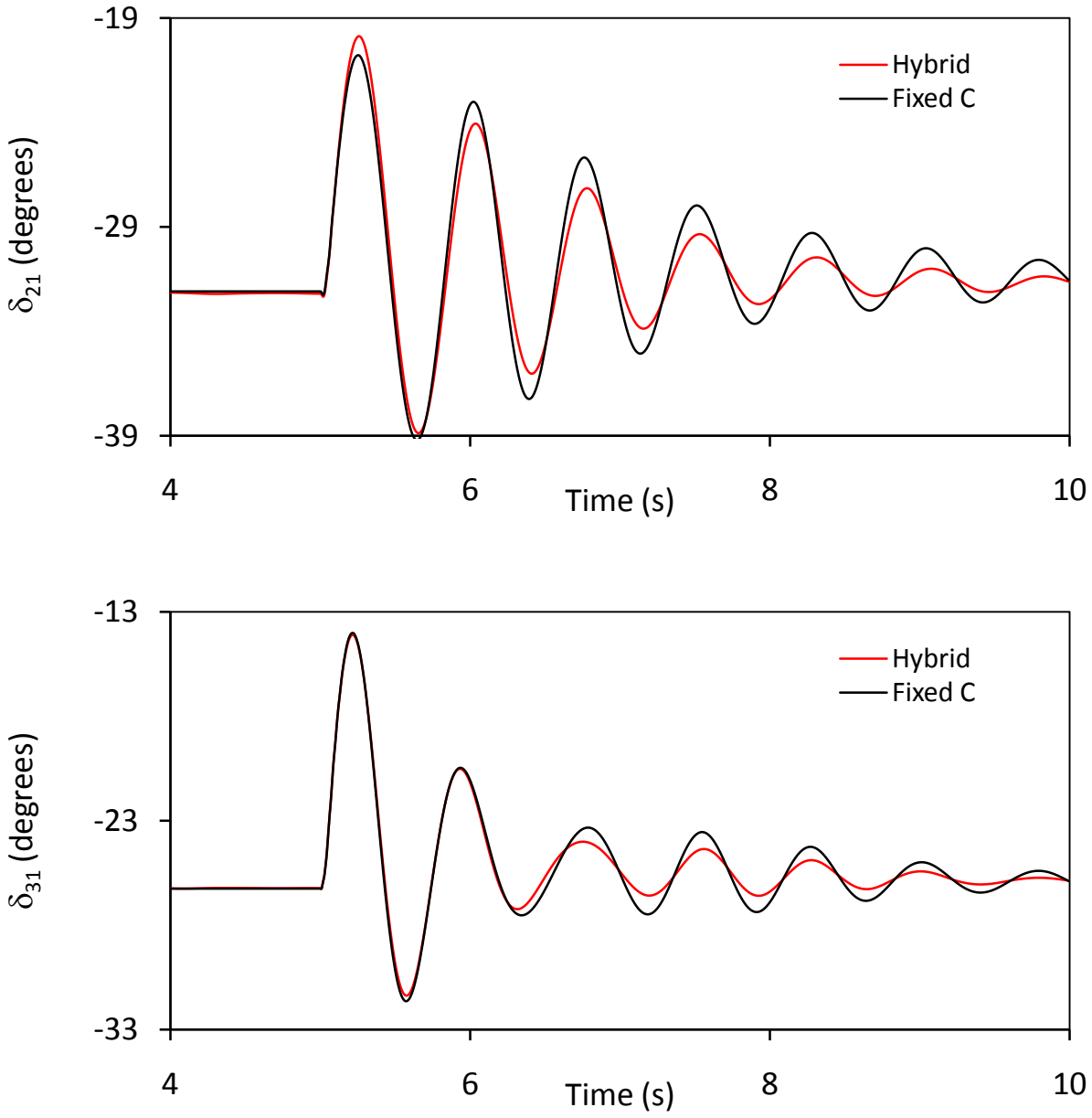


Figure 4.12: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 5 (Case Study II).

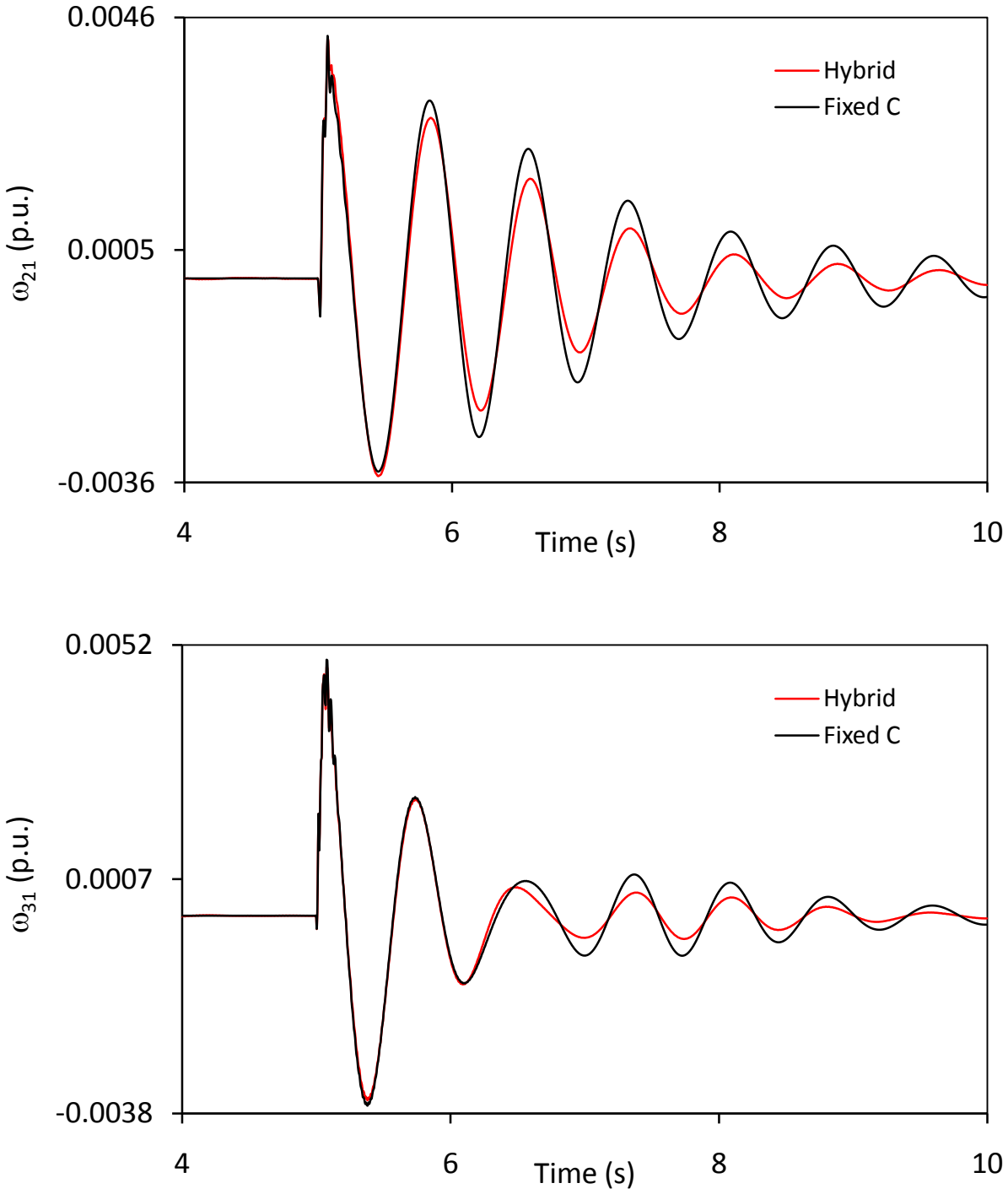


Figure 4.13: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 5 (Case Study II).

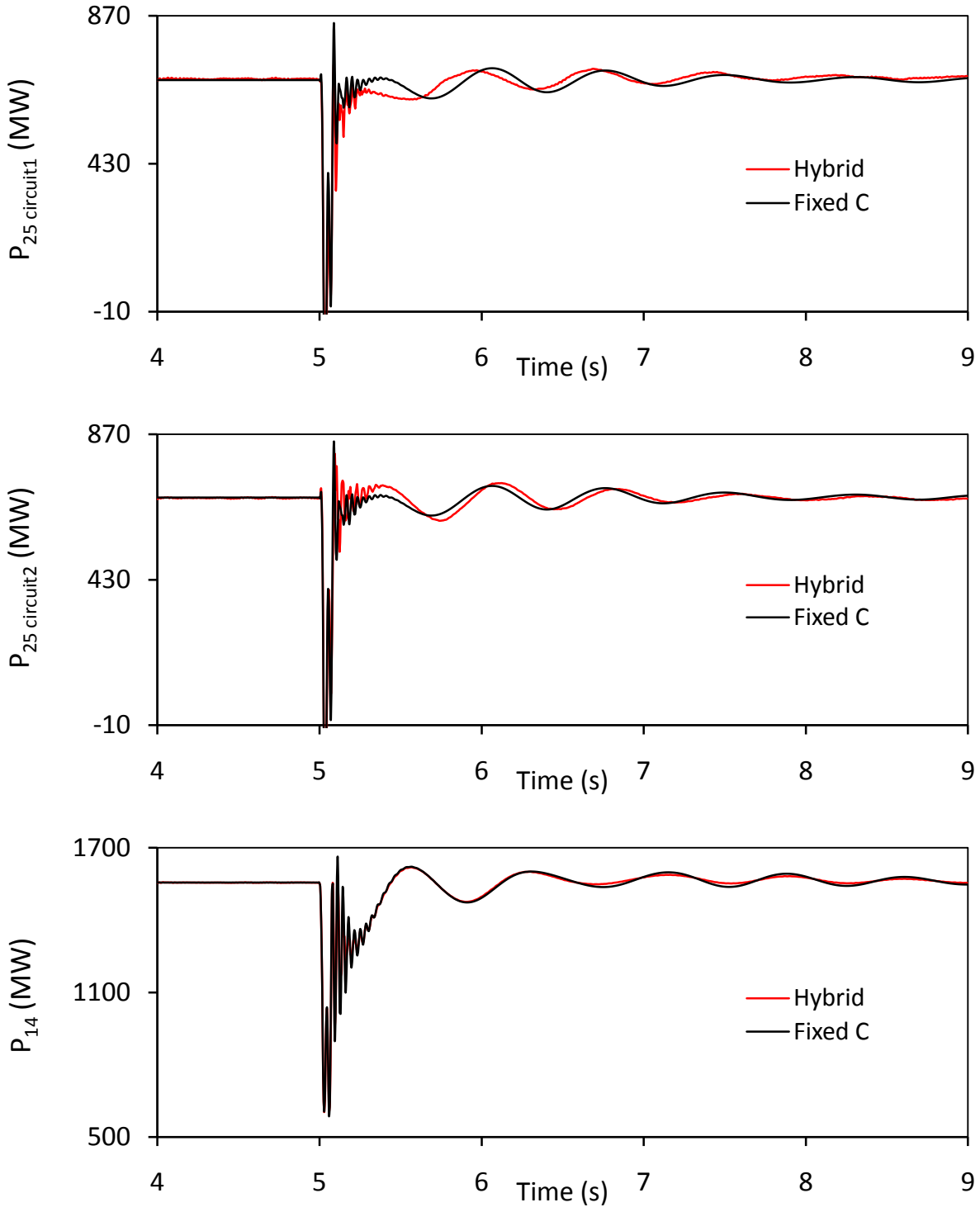


Figure 4.14: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 5 (Case Study II).

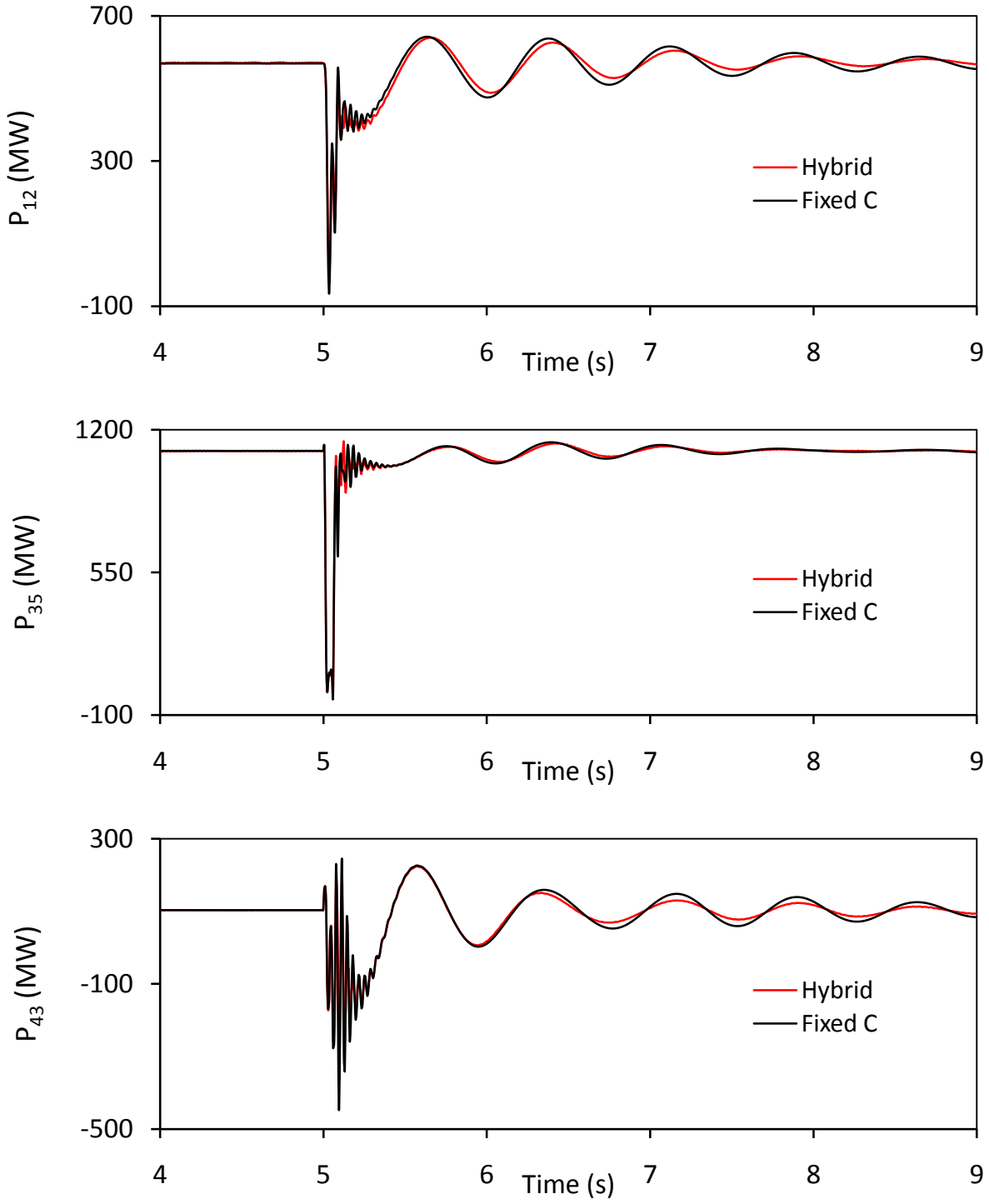


Figure 4.14: continued.

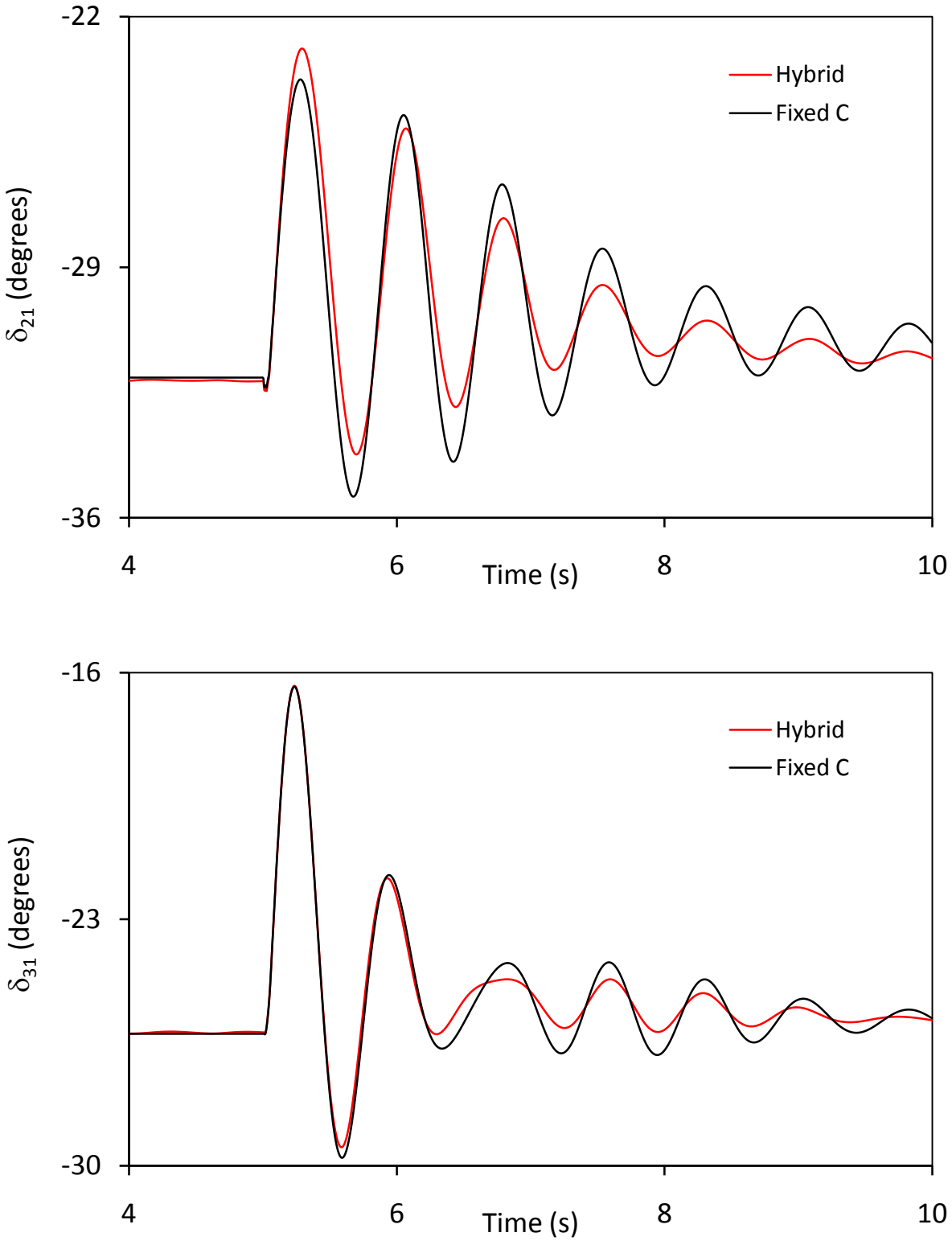


Figure 4.15: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 2 (Case Study II).

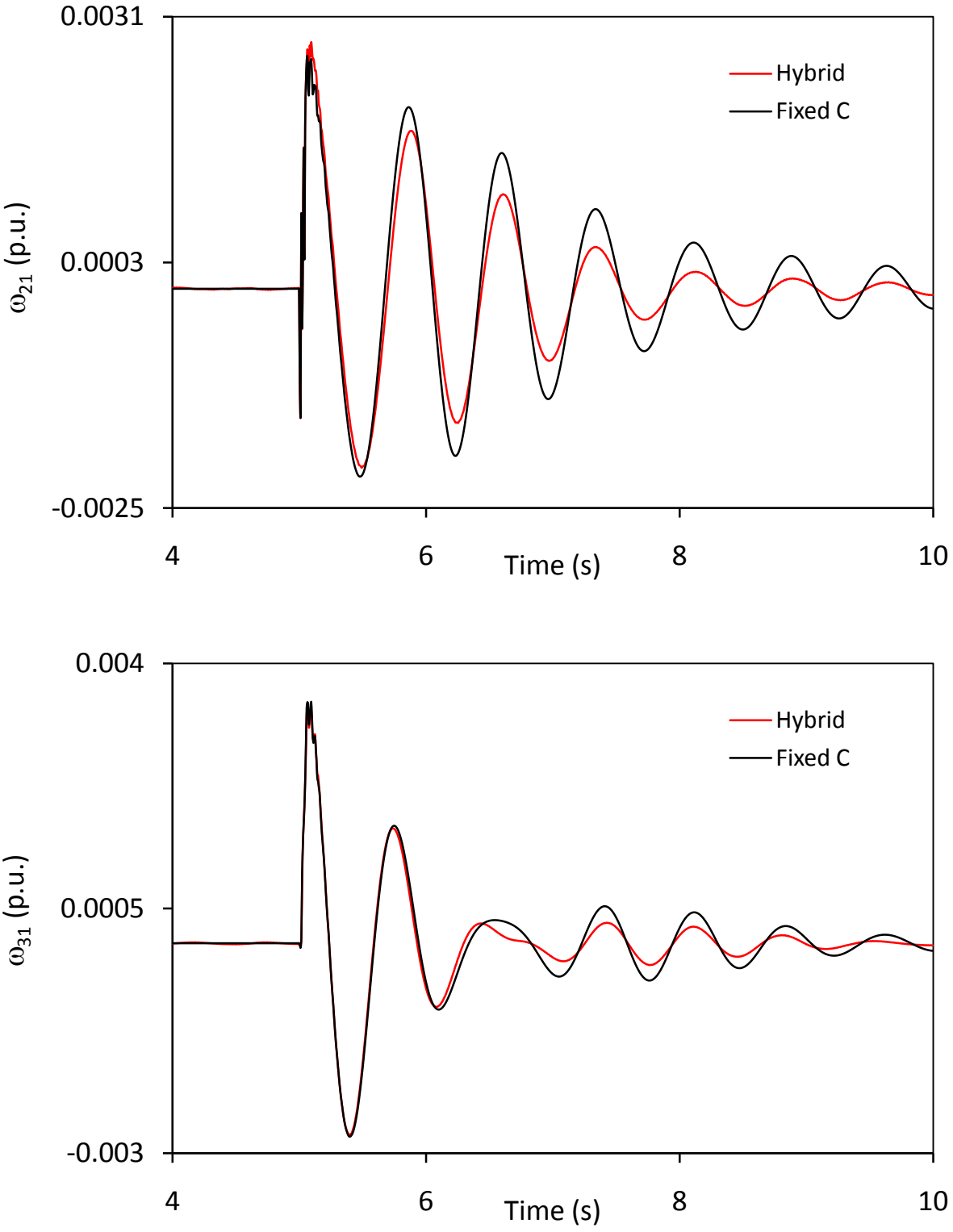


Figure 4.16: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 2 (Case Study II).

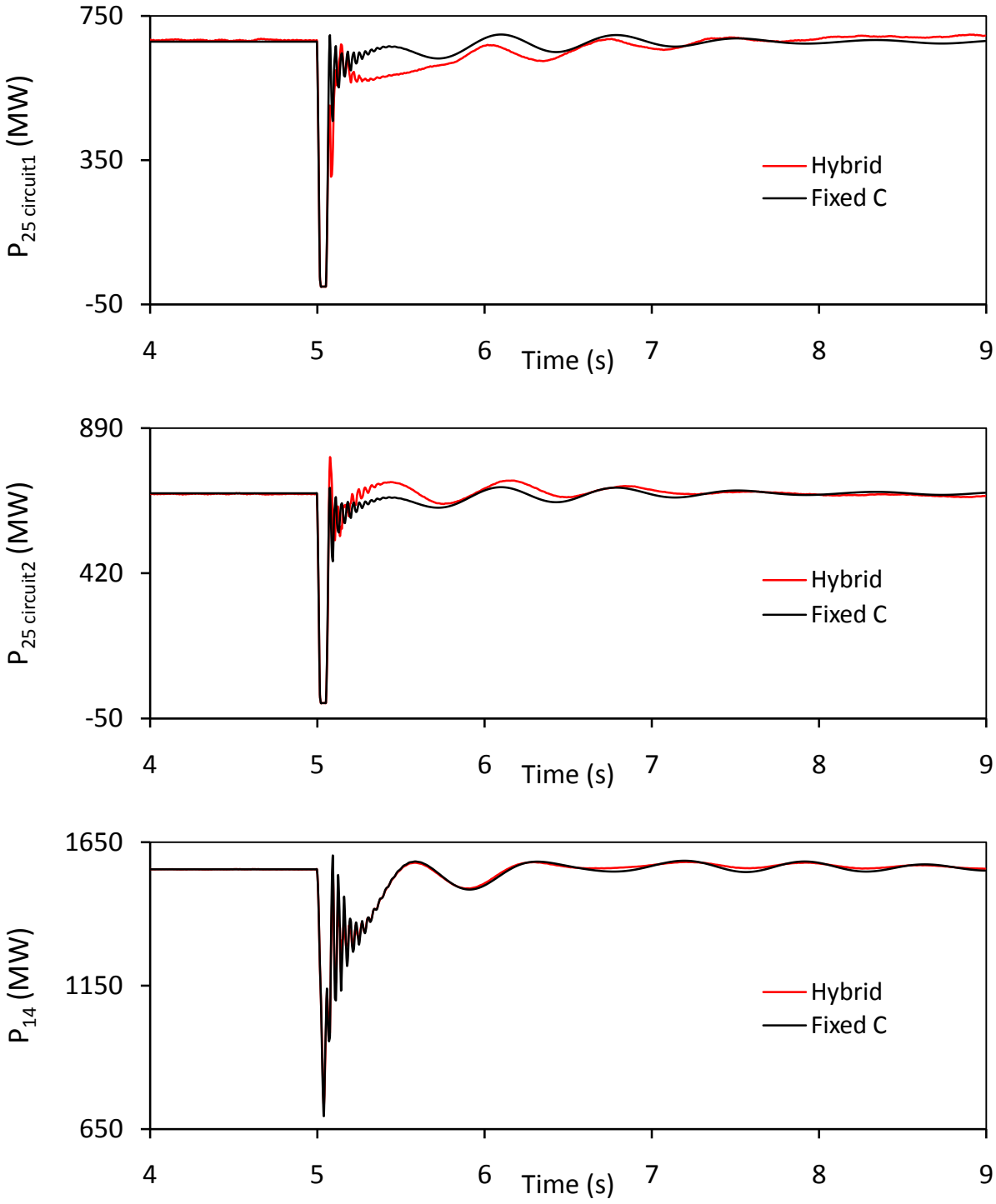


Figure 4.17: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 2 (Case Study II).

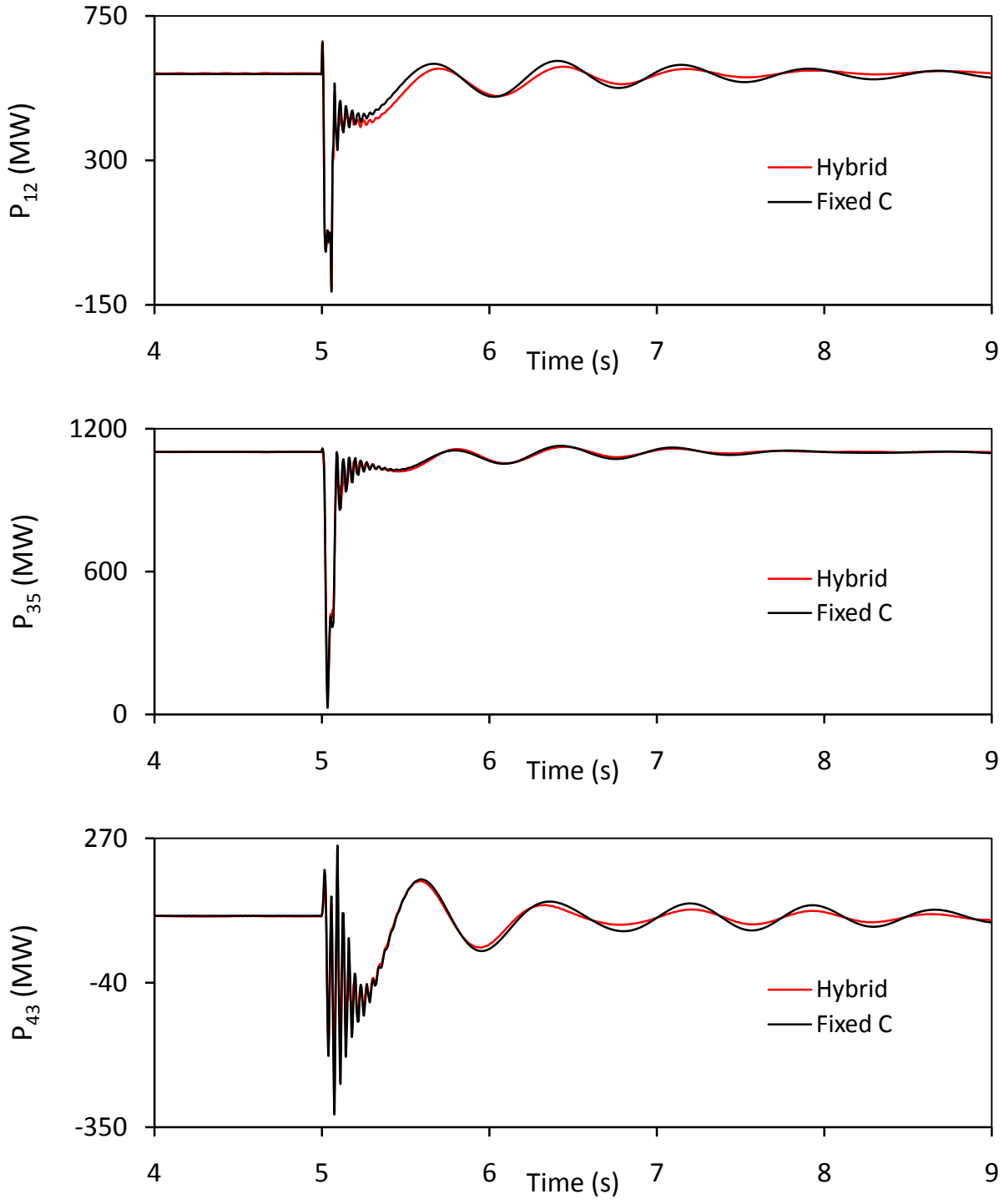


Figure 4.17: continued.

4.5 Case Study III: The Hybrid Single-Phase-SSSC Compensation Scheme is Installed in both Circuits of Line L_1

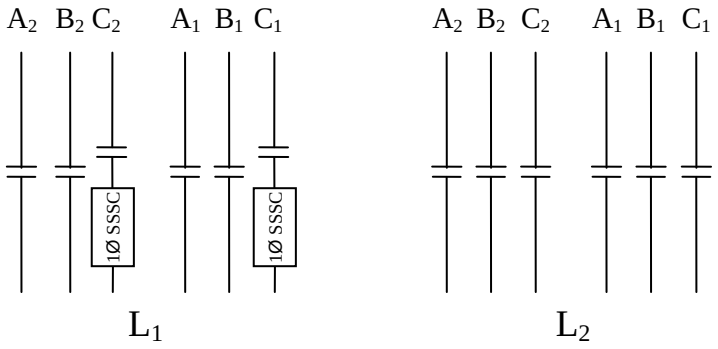


Figure 4.18: Case Study III: The hybrid single-phase-SSSC compensation scheme is installed in both circuits of Line L_1.

Each SSSC provides 50% of the total capacitive compensation and the stabilizing signal is δ_{21} for both controllers. The generator load angles and speeds, measured with respect to generator 1 load angle and speed, and the transmission line real power flow responses during and after clearing a three-cycle, three-phase fault at bus 4 are illustrated in Figures 4.19 to 4.21 for the case when the SSSC supplemental controllers are of a proportional type with a transfer function:

$$G_{P-\delta_{21}}(s) = 0.2\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{4.5}$$

The level of the dynamic capacitive compensation provided by the SSSCs is twice of that in Case Study I. As a result, there are some reductions in the first swings as shown in Figure 4.19. In general, a reduction in the first swing is an indication of an enhancement in the transient stability of the system. It can also be seen from Figures 4.19 and 4.20 that the hybrid single-phase-SSSC scheme is effective in damping the subsequent swings with a better damping than in the case of fixed capacitor compensation.

The effect of the input signal on damping the low frequency oscillations is examined through the use of two new signals, namely the relative deviation between generators 2 and 1 speeds, ω_{21} and the deviation in the real power flow in line L_1, P_{L1}. Satisfactory system transient responses and damping is achievable with either signal. The possibility of using a different

controller for each signal was explored. This resulted in designing controllers with the transfer functions (for ω_{21} and for P_{L1}) is given respectively, in Equations 4.6 and 4.7.

$$G_{P-\omega_{21}}(s) = -200\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{4.6}$$

$$G_{P-P_{L1}}(s) = 0.1\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{4.7}$$

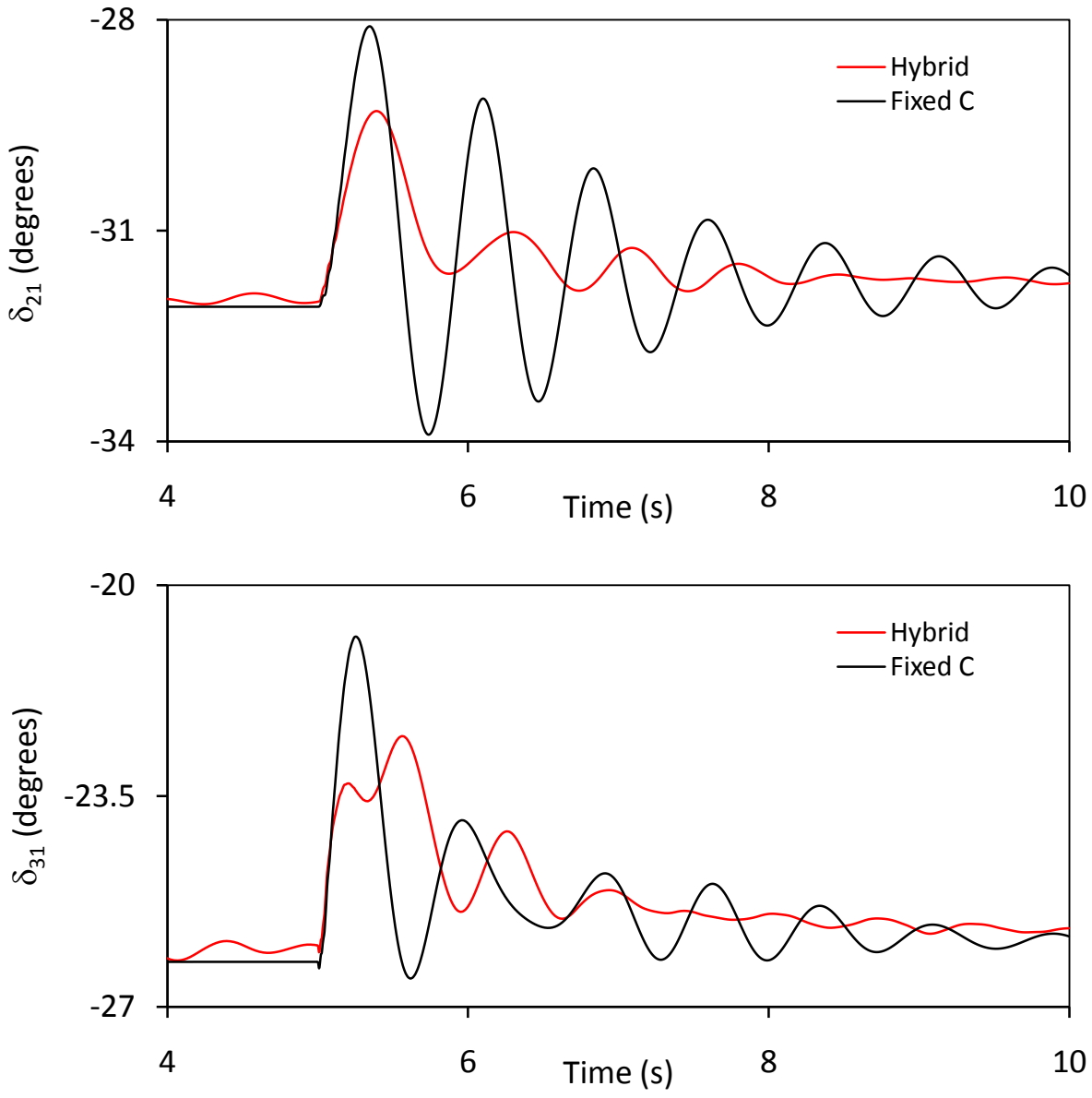


Figure 4.19: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study III).

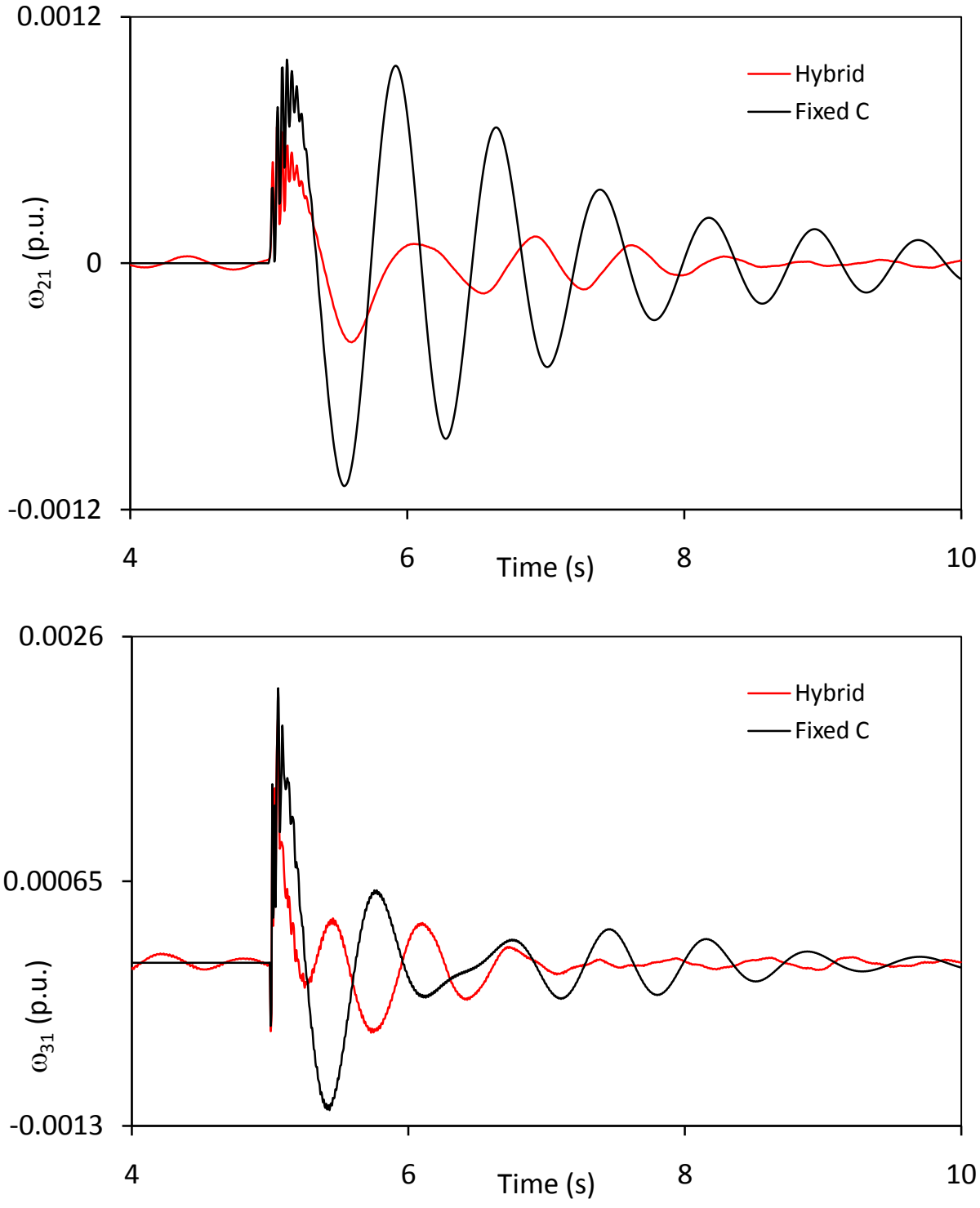


Figure 4.20: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study III).

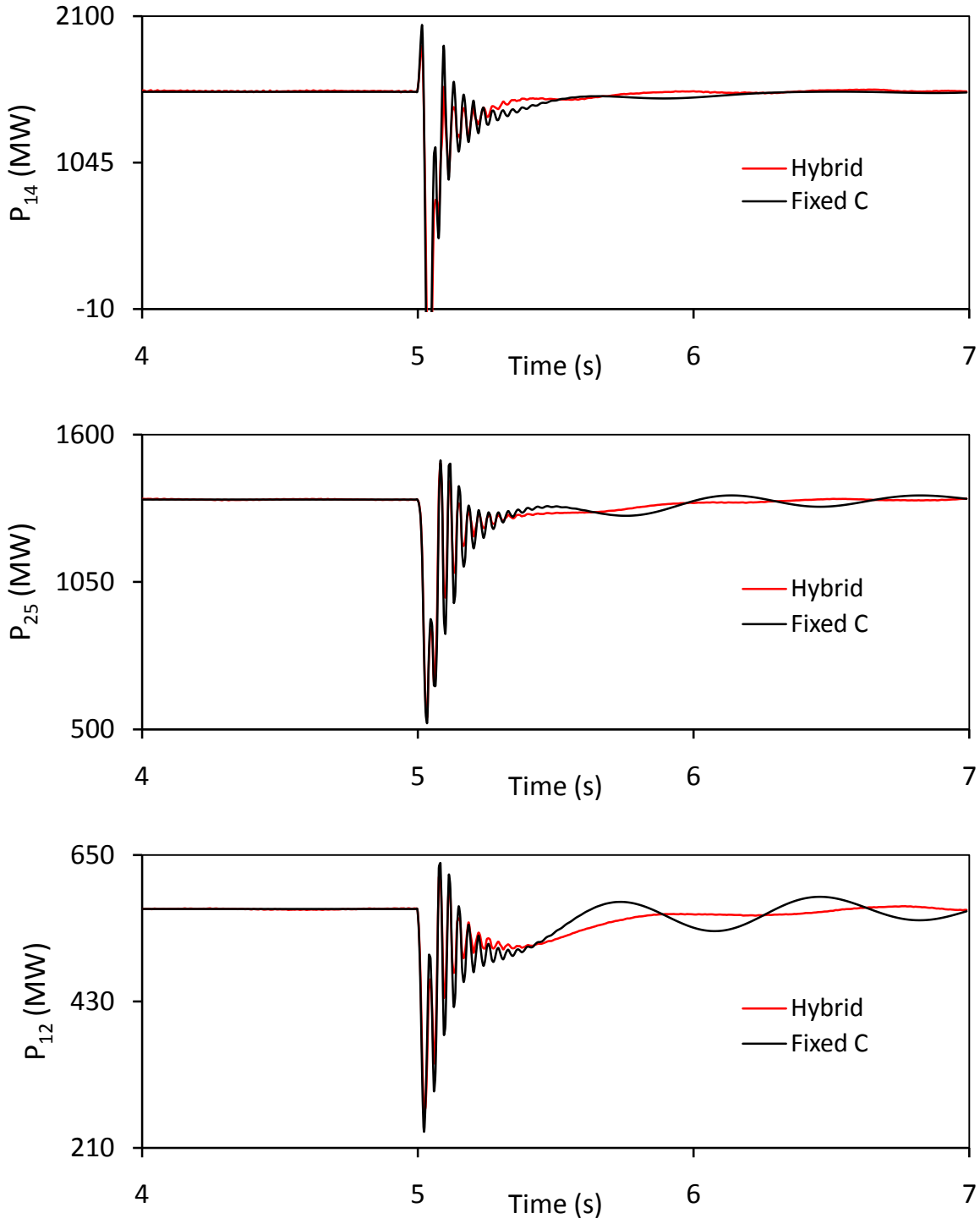


Figure 4.21: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study III).

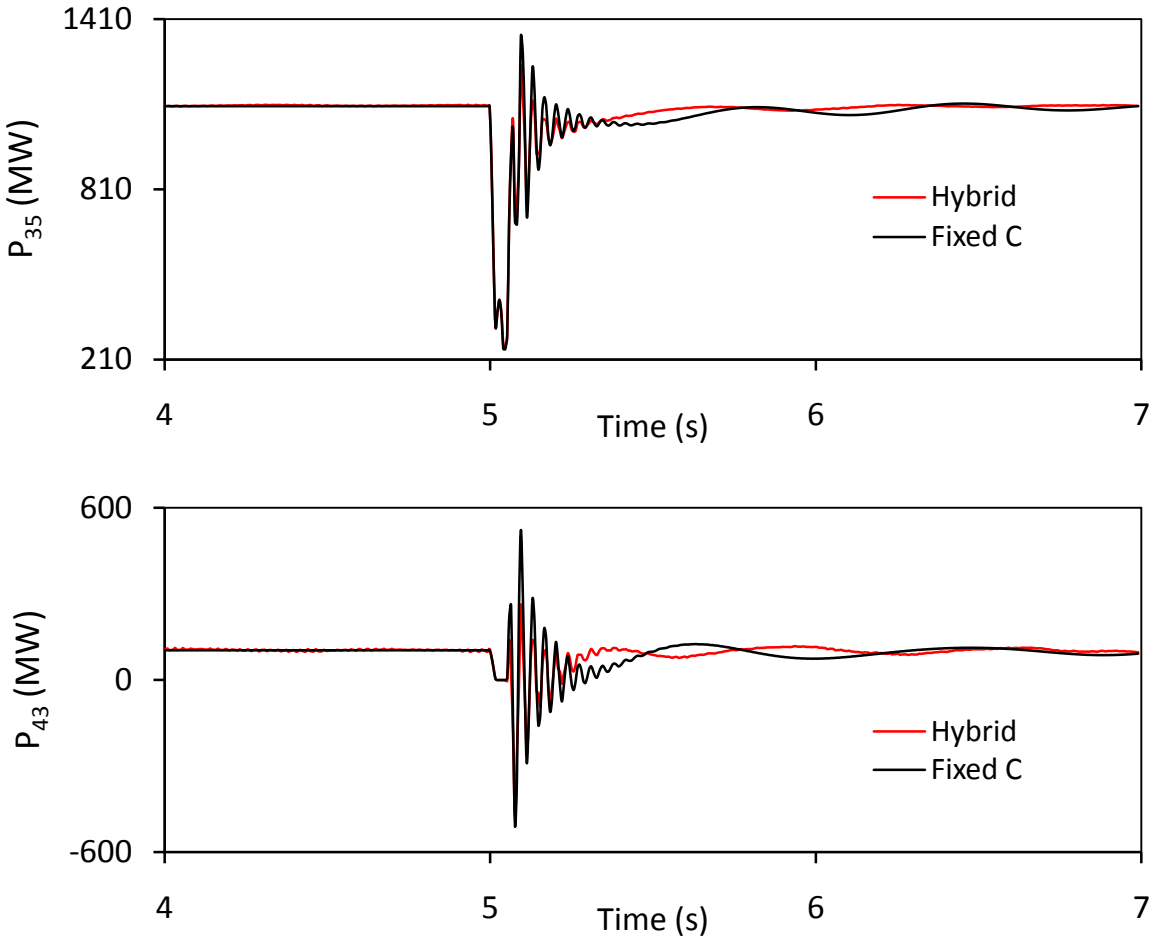


Figure 4.21: continued.

A comparison between the system responses to the three controllers is shown in Figure 4.22. It can be seen from this figure that the system transient responses in the three cases are comparable. The response in the case of the input signal δ_{21} is still relatively the best, especially near steady-state. This should be expected due to the direct relationship between the relative load angles and the generators that yield the problem.

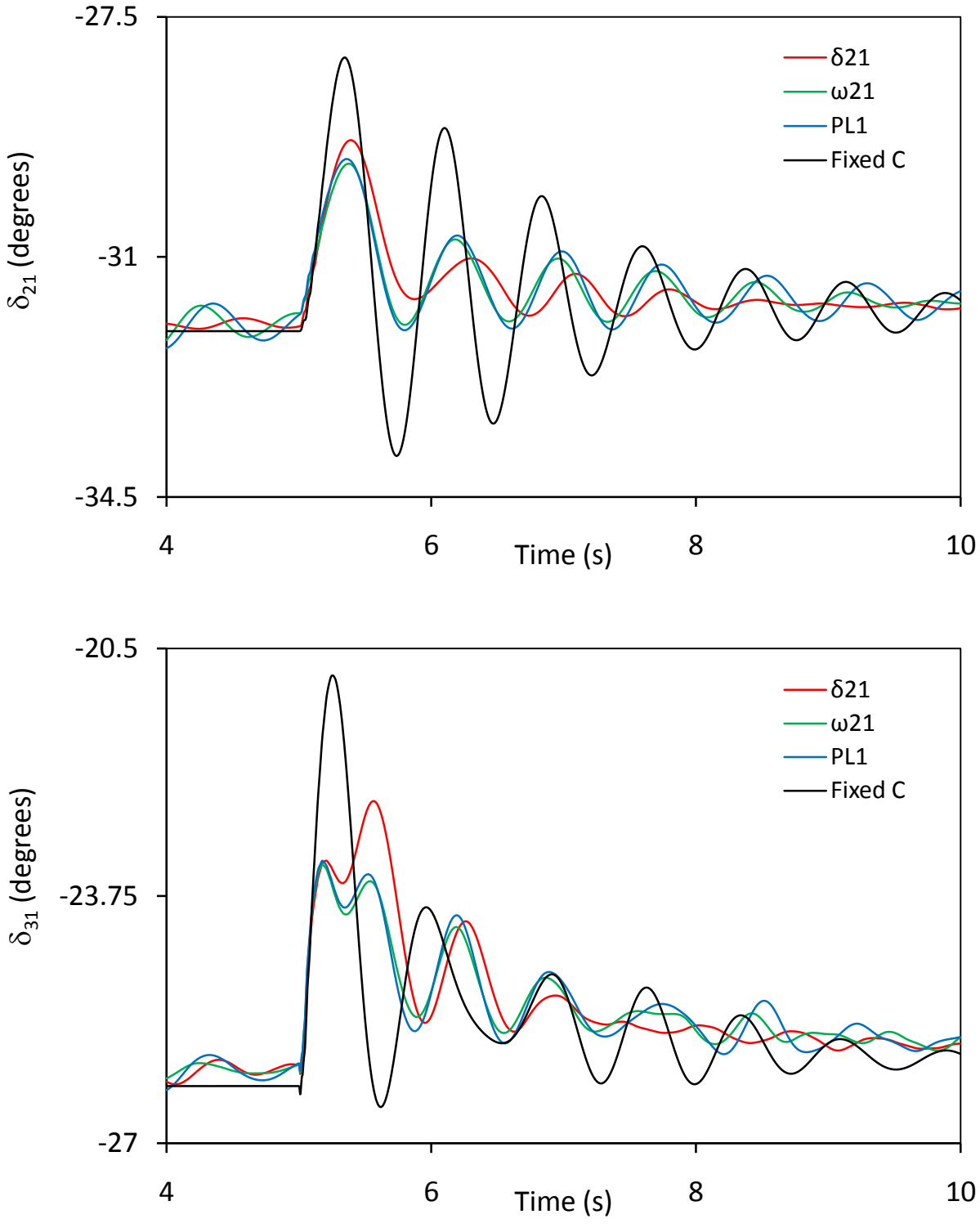


Figure 4.22: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study III, effect of the stabilizing signal).

4.6 Case Study IV: The Hybrid Single-Phase-SSSC Compensation Scheme is Installed in all Circuits of Lines L_1 and L_2

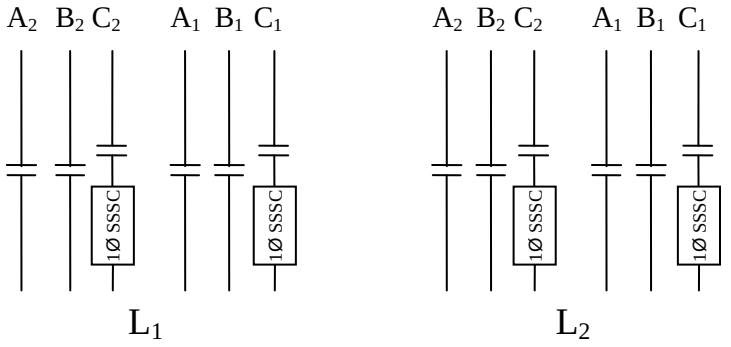


Figure 4.23: Case Study IV: The hybrid single-phase-SSSC compensation scheme is installed in all circuits of lines L_1 and L_2.

Each SSSC provides 50% of the total capacitive compensation and the disturbance is a three-cycle, three-phase fault at bus 4. Four different combinations of stabilizing signals (tabulated in Table 4.1) are examined in order to determine the combination that would result in the best system transient time responses. The final results of the time-domain simulation studies (controllers tuning) are shown in Figure 4.24 which illustrates the generator load angles, measured with respect to generator 1 load angle, during and after fault clearing. The transfer functions of the SSSC supplemental controllers for the four combinations are given in Table 4.2.

Table 4.1: The four examined combinations of stabilizing signals.

Combination	Each SSSC in L_1	Each SSSC in L_2
1	δ_{21}	δ_{21}
2	δ_{31}	δ_{21}
3	δ_{31}	P_{L2}
4	P_{L1}	δ_{21}

It can be seen from Figure 4.24 that the best damping of the relative load angle responses are achieved with the δ_{31}- δ_{21} combination. The second best damped responses are obtained with the δ_{21}- δ_{21} combination. Again, these results should be expected due to the direct relationship between the relative load angles and the generators that yield the problem.

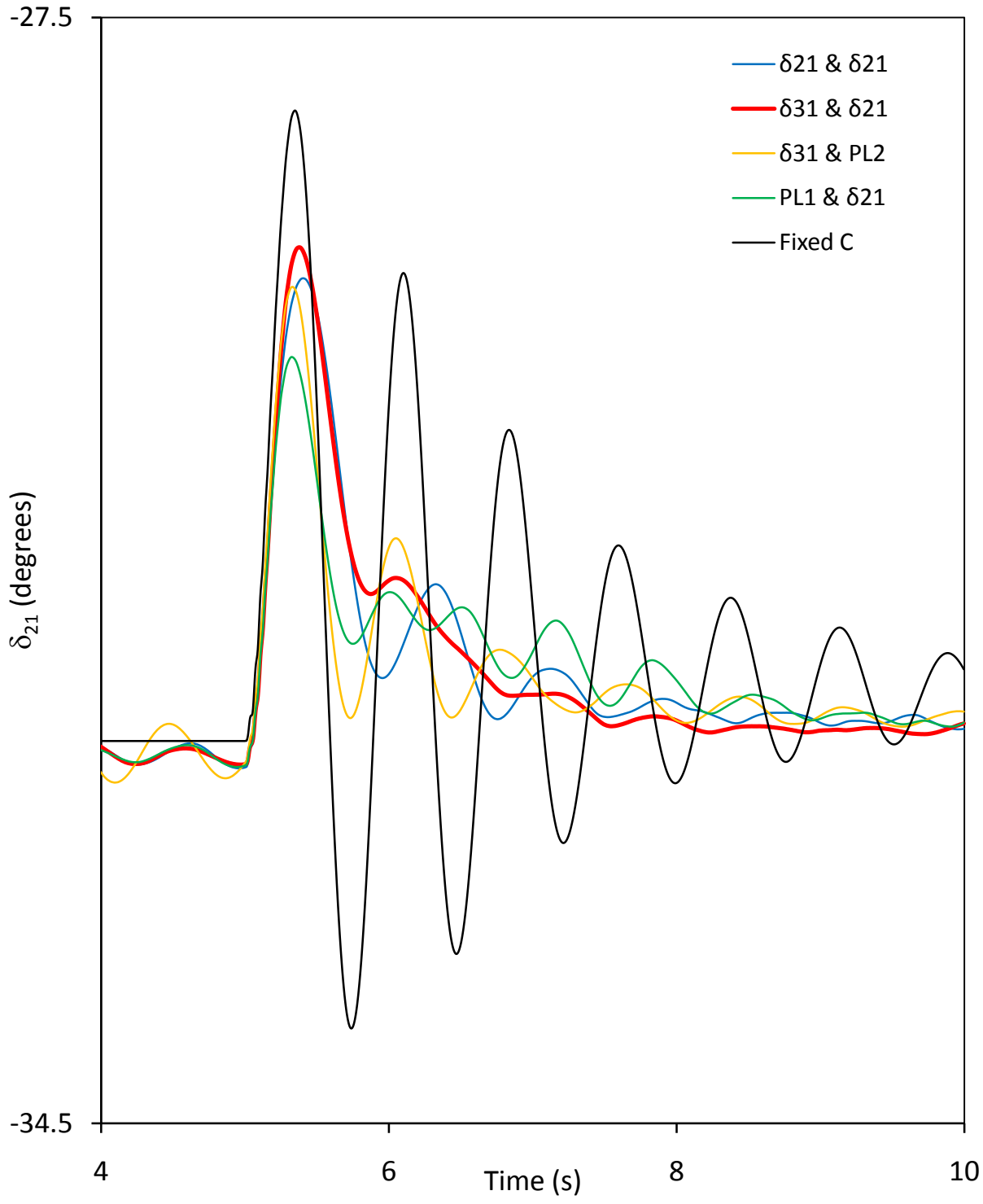


Figure 4.24: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV).

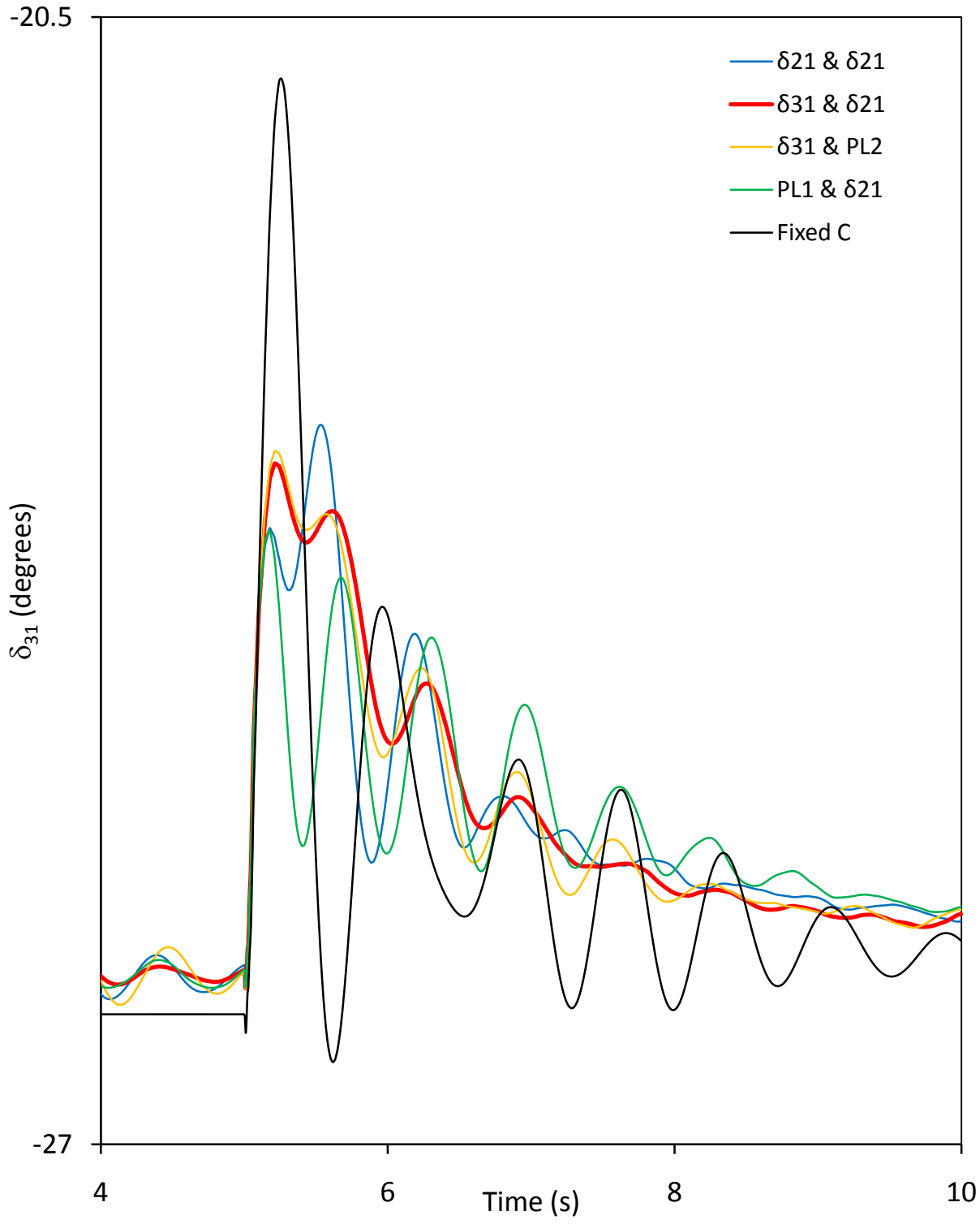


Figure 4.24: Continued.

Table 4.2: Transfer functions of the SSSC supplemental controllers.

Combination	Each SSSC in L_1	Each SSSC in L_2
1	$G(s) = 0.05\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
2	$G(s) = 0.1\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
3	$G(s) = 0.1\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
4	$G(s) = 3.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$

Having established that δ_{31}- δ_{21} are the best stablizing input signals, Figures 4.25 and 4.26 illustrate respectively, the transient time responses of the generator speeds (relative to the speed of generator 1) and the real power flow on the five transmission lines. The variations of the SSSC modulated reactances are shown in Figures 4.27 and 4.28.

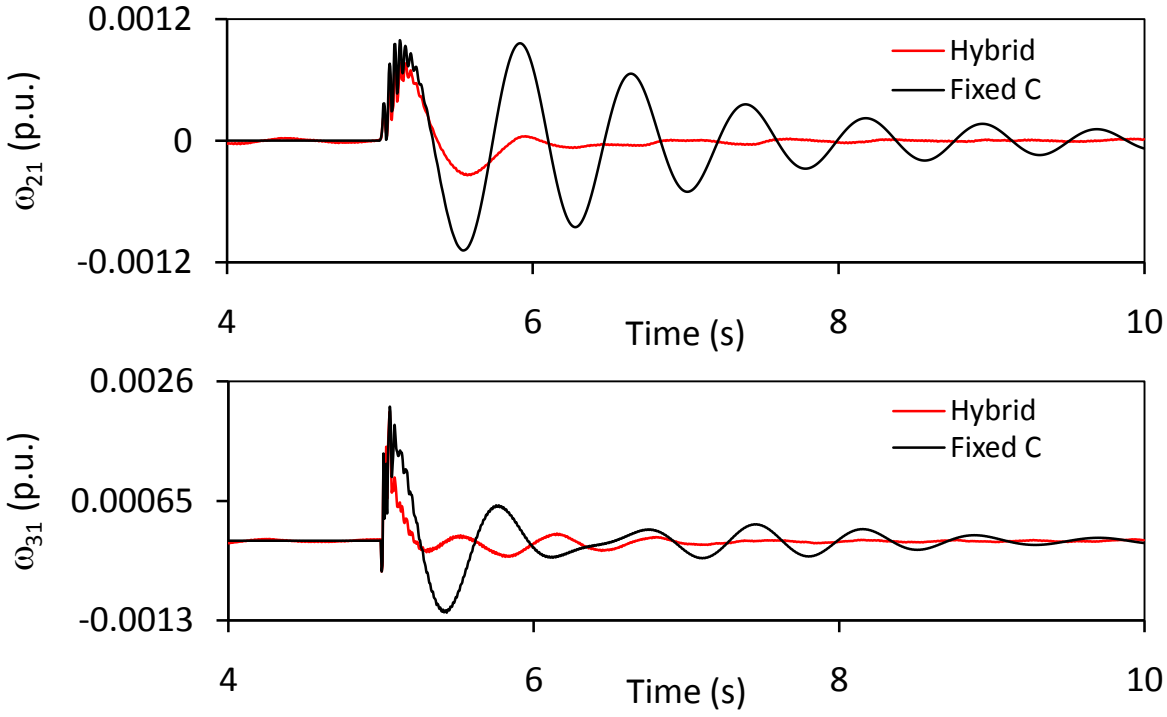


Figure 4.25: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV, input signals are δ_{31} and δ_{21}).

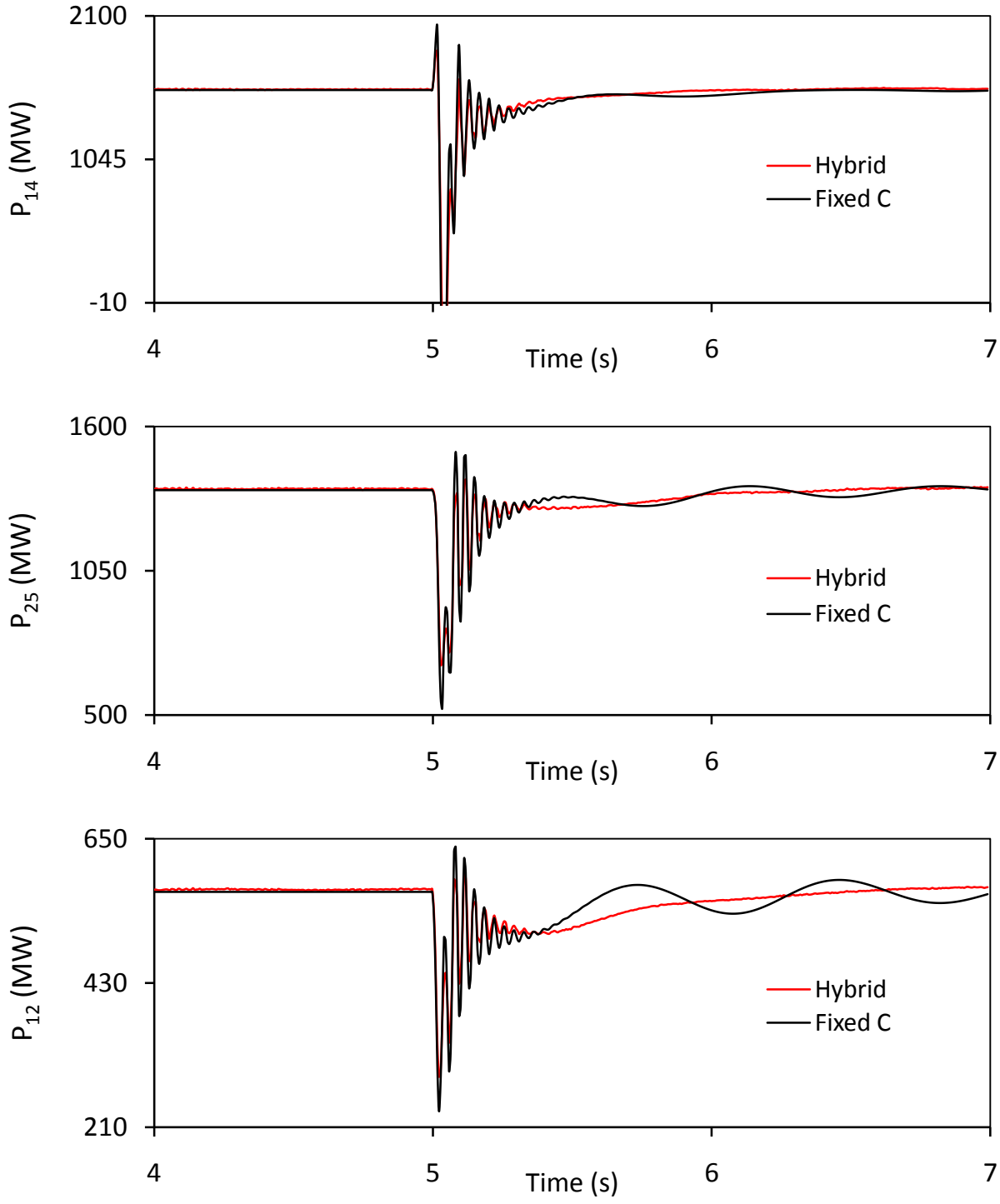


Figure 4.26: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV, input signals are δ_{31} and δ_{21}).

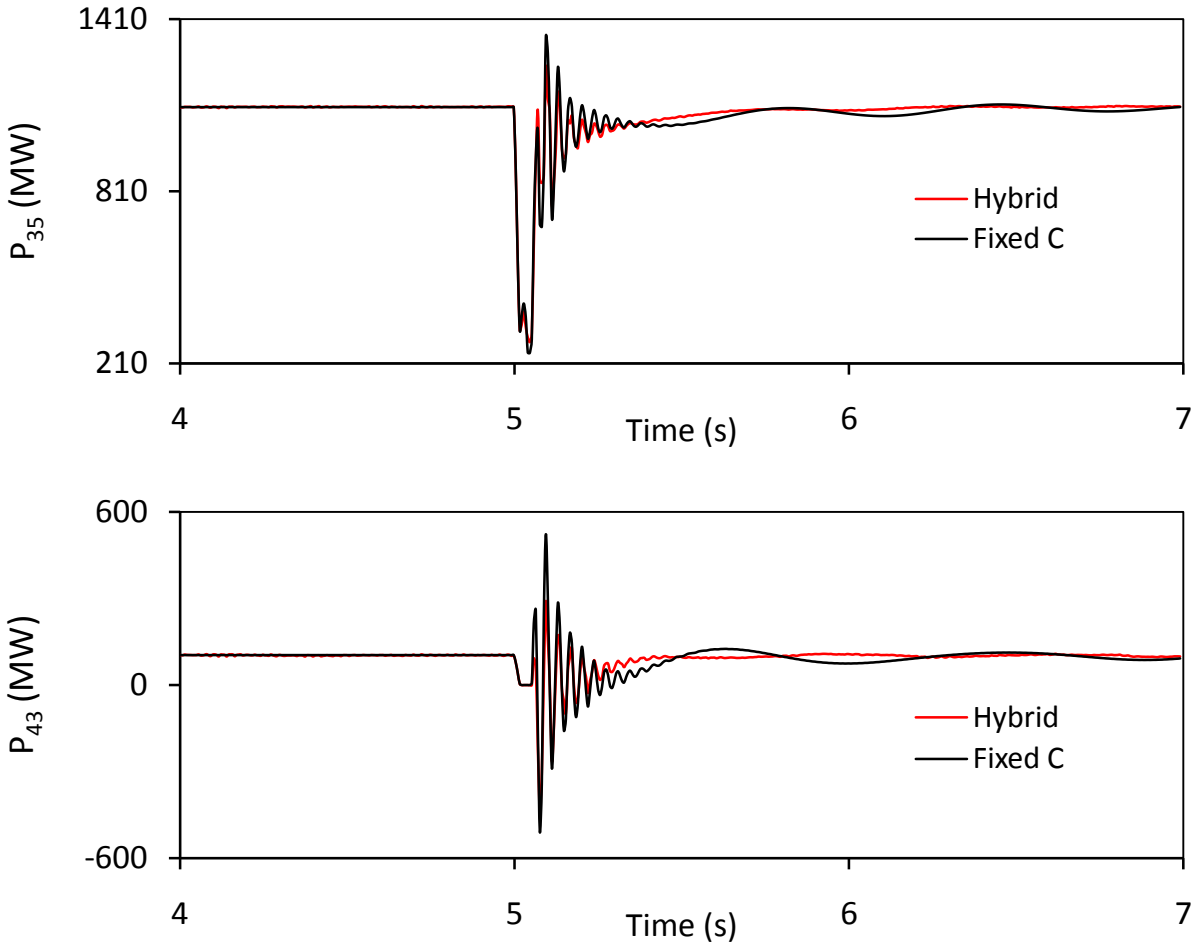


Figure 4.26: Continued.

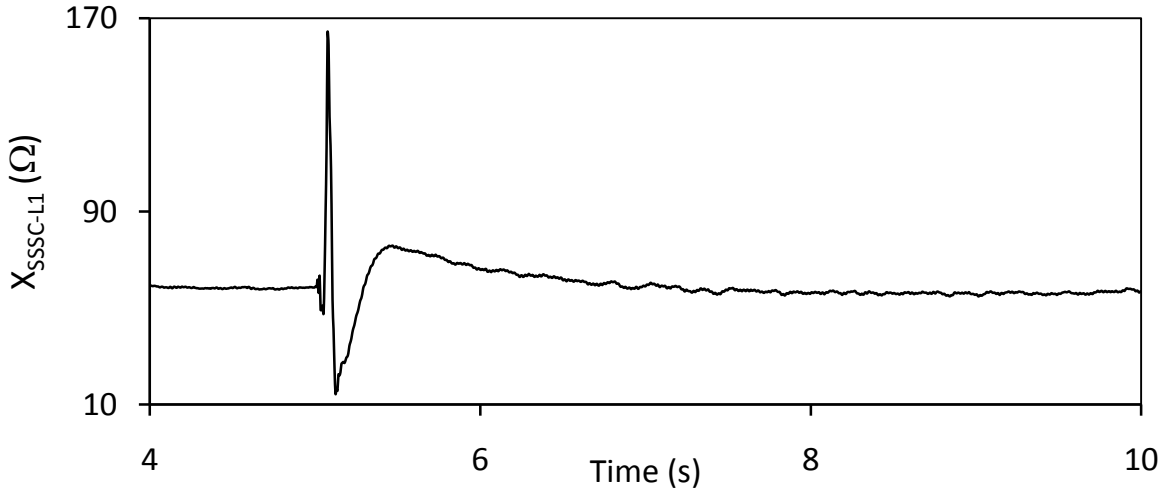


Figure 4.27: Variations of line L_1 SSSC reactances during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV, input signals are δ_{31} and δ_{21}).

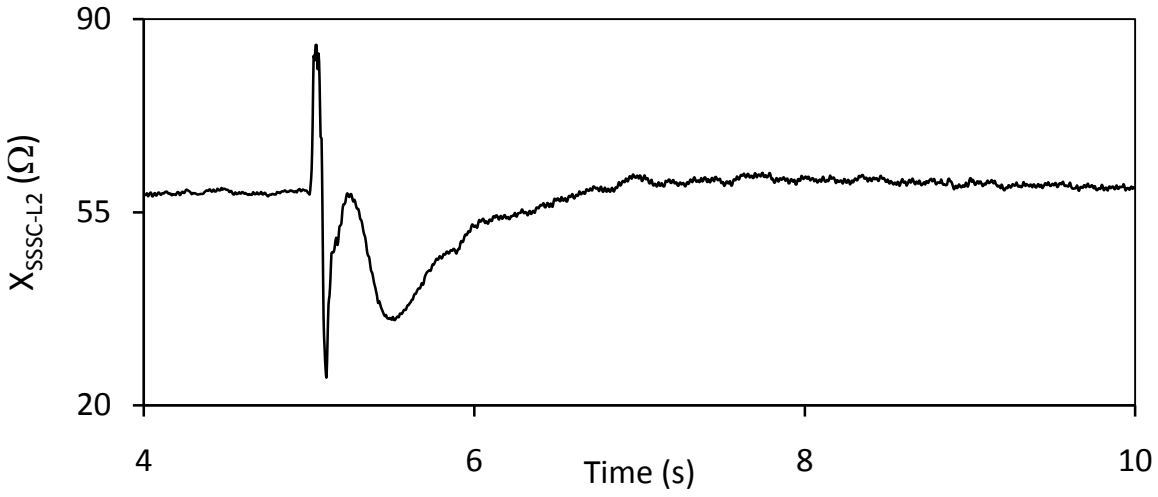


Figure 4.28: Variations of line L_2 SSSC reactances during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV, input signals are δ_{31} and δ_{21}).

4.6.1 Performance of the scheme at a different loading profile

Each SSSC provides 50% of the total capacitive compensation and the stabilizing signals are δ_{31} for SSSCs in L_1 and δ_{21} for SSSCs in L_2. Moreover, the disturbance is a three-cycle, three-phase fault at bus 4. Load S_1 is increased by 600 MW while load S_2 is reduced by the same amount. The power flow results for the bus voltages and the line real power flows of the system under study are shown in Figure 4.29. The comparison between this figure and Figure 2.6 shows that the direction of the real power flow between buses 4 and 3 is reversed.

Figure 4.30 illustrates the generator load angles, measured with respect to generator 1 load angle, during and after fault clearing. The transfer functions of the SSSC supplemental controllers are given in Table 4.3. It can be seen from Figure 4.30 that, at this loading condition, the hybrid single-phase-SSSC scheme provides again a better damping performance to system oscillations compared to fixed capacitor compensation.

Table 4.3: Transfer functions of the SSSC supplemental controllers with the stabilizing signals δ_{31} for SSSCs in L_1 and δ_{21} for SSSCs in L_2.

Each SSSC in L_1	Each SSSC in L_2
$G(s) = 0.2\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G(s) = -0.05\frac{15}{(s+15)}\frac{2s}{(2s+1)}$

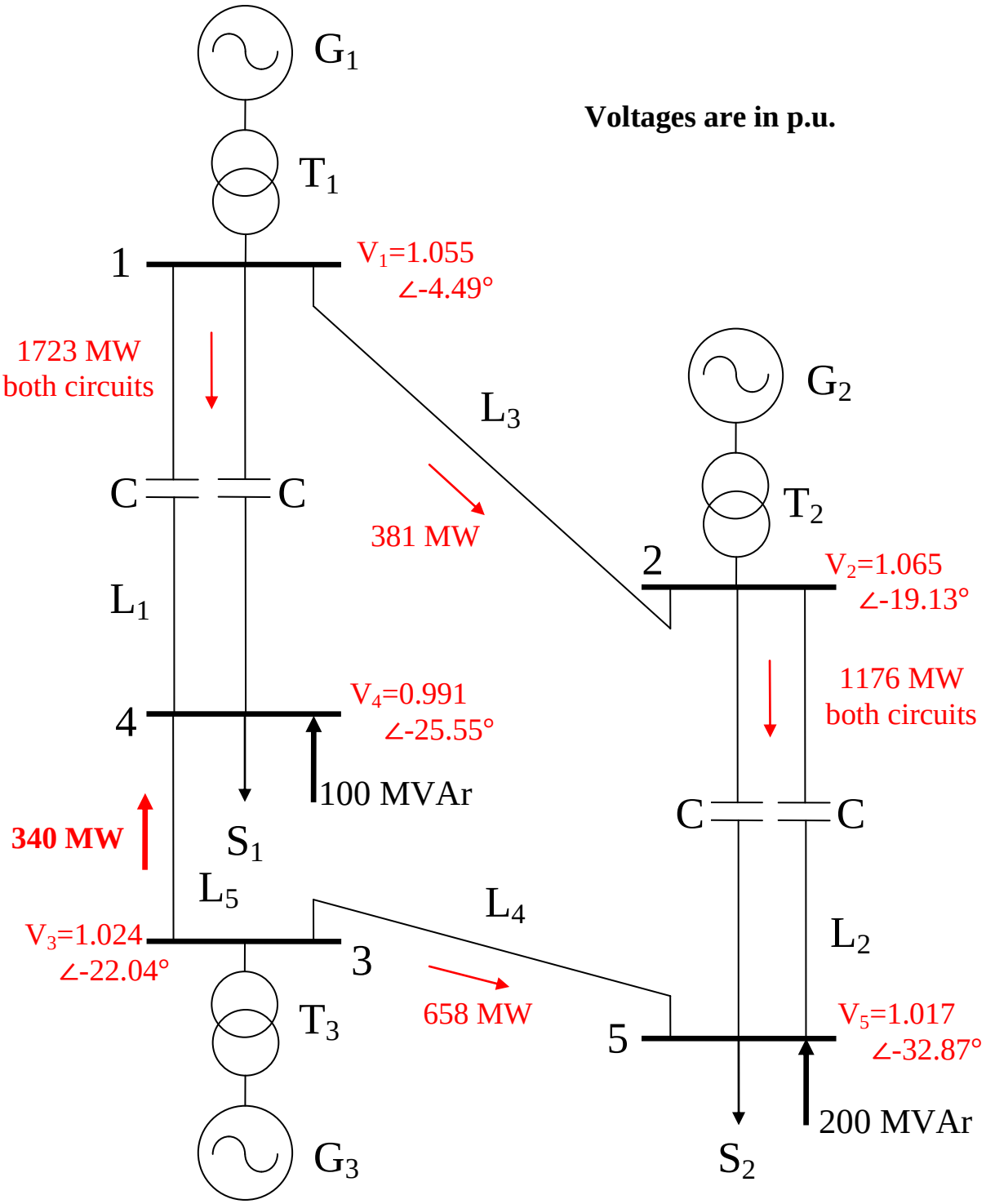


Figure 4.29: Power flow results of bus voltages and line real power flows of the system under the study.

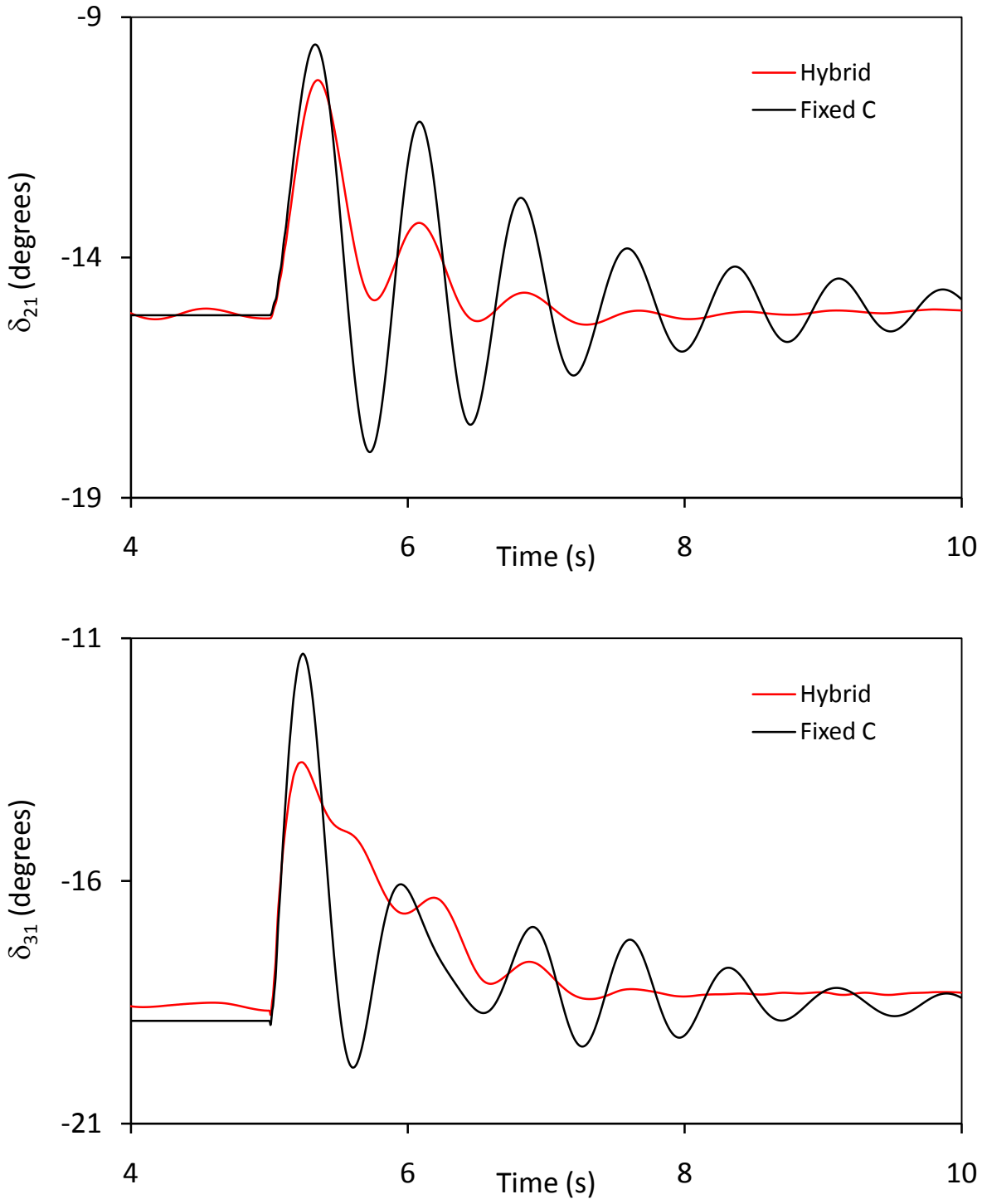


Figure 4.30: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV at a different loading profile, stabilizing signals: δ_{31} for SSSCs in L_1 and δ_{21} for SSSCs in L_2).

4.6.2 Performance of a dual-channel SSSC supplemental controller

Any one of the four signals, δ_{21}, δ_{31}, P_{L1}, and P_{L2} contains the system's two natural modes of oscillations and can be used to add damping to these modes as it has been demonstrated in Sections 4.3 to 4.6. The sum of two properly selected signals, however, should result in a more effective damping. The reason is that the two natural modes of oscillations are, in general, not in phase. A dual-channel controller would adjust separately the gain and phase of each mode of oscillations and, thus, provides a better damping. The performance of the dual-channel SSSC supplemental controller shown in Figure 4.31 in damping power system oscillations is examined using the six pairs of signals given in Table 4.4. It is assumed again that each SSSC provides 50% of the total capacitive compensation and that the disturbance is a three-cycle, three-phase fault at bus 4. Moreover, investigations are conducted on the system with the pre-fault load flow in Figure 4.29.

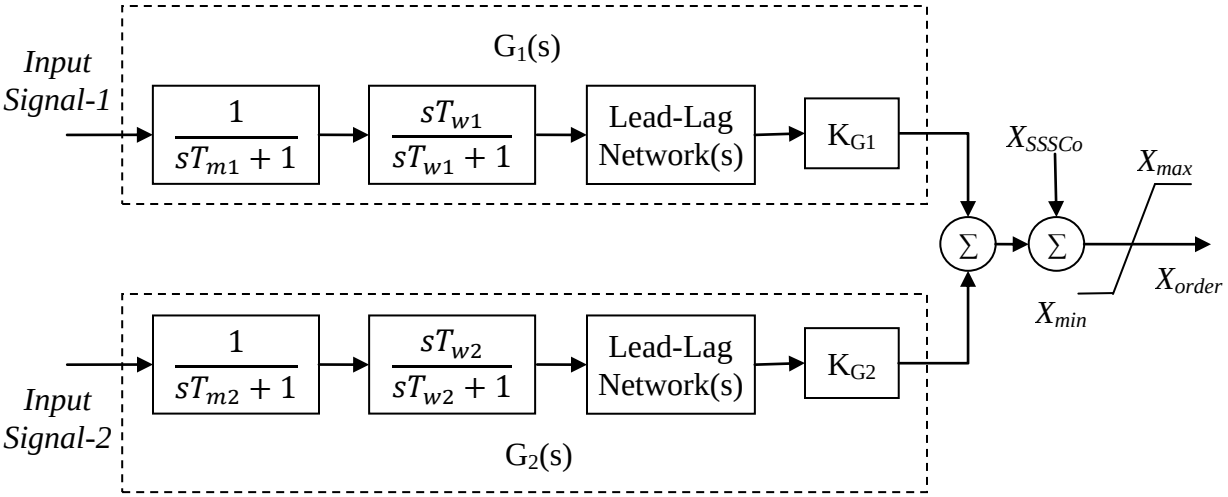


Figure 4.31: Structure of a dual-channel POD controller.

The final results of the time-domain simulation studies (controllers tuning) are shown in Figure 4.32 which illustrates the generator load angles, measured with respect to generator 1 load angle, during and after fault clearing. These results (in red color) are compared to the hybrid case of Figure 4.30. The transfer functions of the SSSC supplemental controllers for the six pairs of signals are given in Table 4.5.

Table 4.4: The six examined combinations of stabilizing signals.

Pair Number	Each SSSC (input signal-1, input signal-2)
1	δ_{21}, δ_{31}
2	δ_{21}, P_{L1}
3	δ_{21}, P_{L2}
4	δ_{31}, P_{L1}
5	δ_{31}, P_{L2}
6	P_{L1}, P_{L2}

Table 4.5: Transfer functions of the dual-channel SSSC supplemental controllers in L_1 and L_2.

Pair Number	Each SSSC in L_1	Each SSSC in L_2
1	$G_1(s) = 0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = 0.02\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G_1(s) = -0.1\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = -0.025\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
2	$G_1(s) = 0.05\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = 0.25\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G_1(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = -3.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
3	$G_1(s) = 0.2\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = 0.1\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G_1(s) = -0.15\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = -7.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
4	$G_1(s) = 0.2\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = 0.05\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G_1(s) = -0.01\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = -3.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
5	$G_1(s) = 0.25\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = 0.1\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G_1(s) = -0.05\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = -7.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$
6	$G_1(s) = 3.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = 0.01\frac{15}{(s+15)}\frac{2s}{(2s+1)}$	$G_1(s) = -1.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$ $G_2(s) = -12.0\frac{15}{(s+15)}\frac{2s}{(2s+1)}$

It can be seen from Figure 4.32 that the best damping of the relative load angle responses are achieved with pair 5 (δ_{31}, P_{L2}). The second and third best damped responses are very close and are obtained with pairs 4 and 3. It can also be seen from Figure 4.32 that the worst damped responses are obtained with pair 6, namely P_{L1}, P_{L2}.

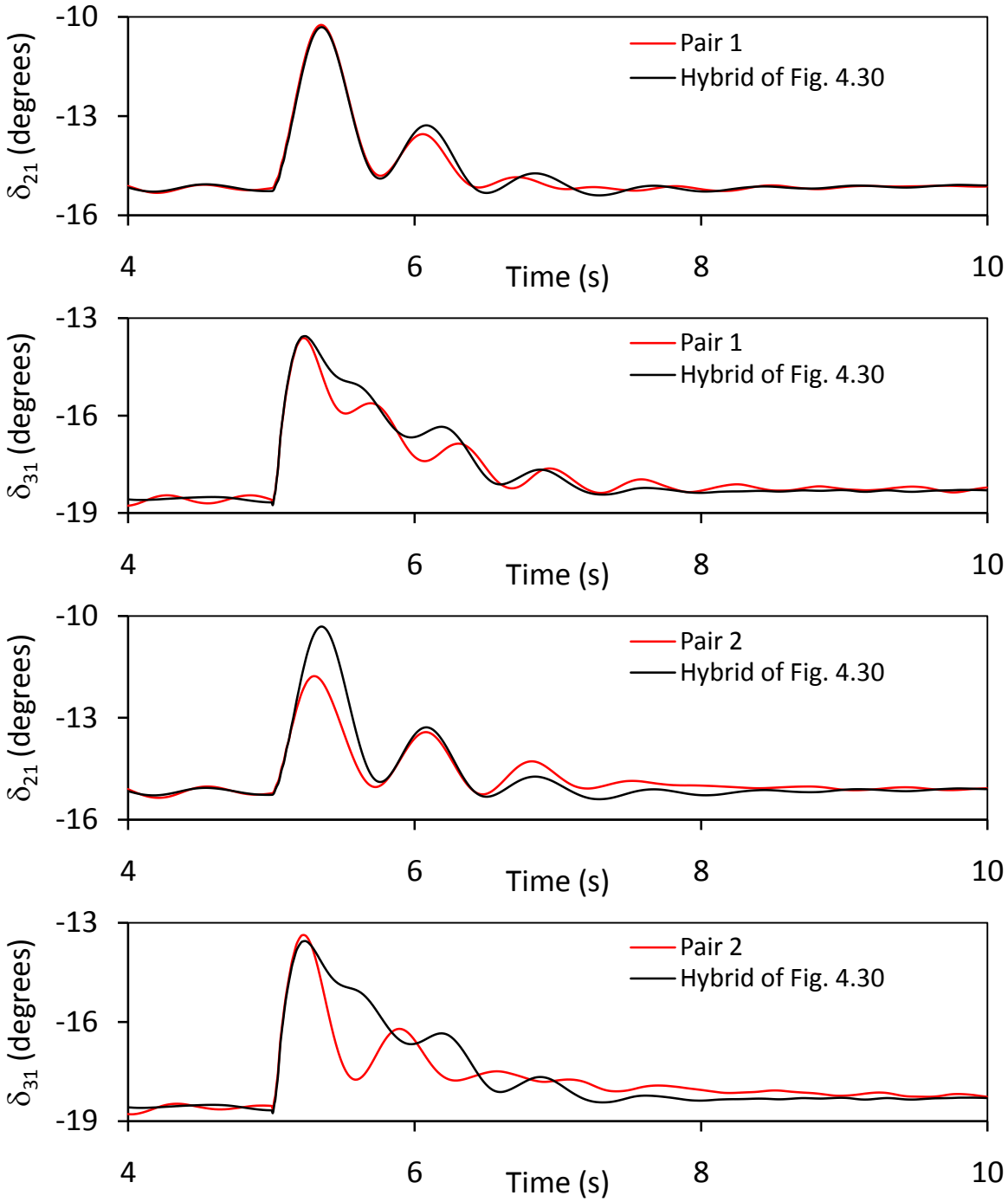


Figure 4.32: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV at a different loading profile, dual-channel supplemental controllers).

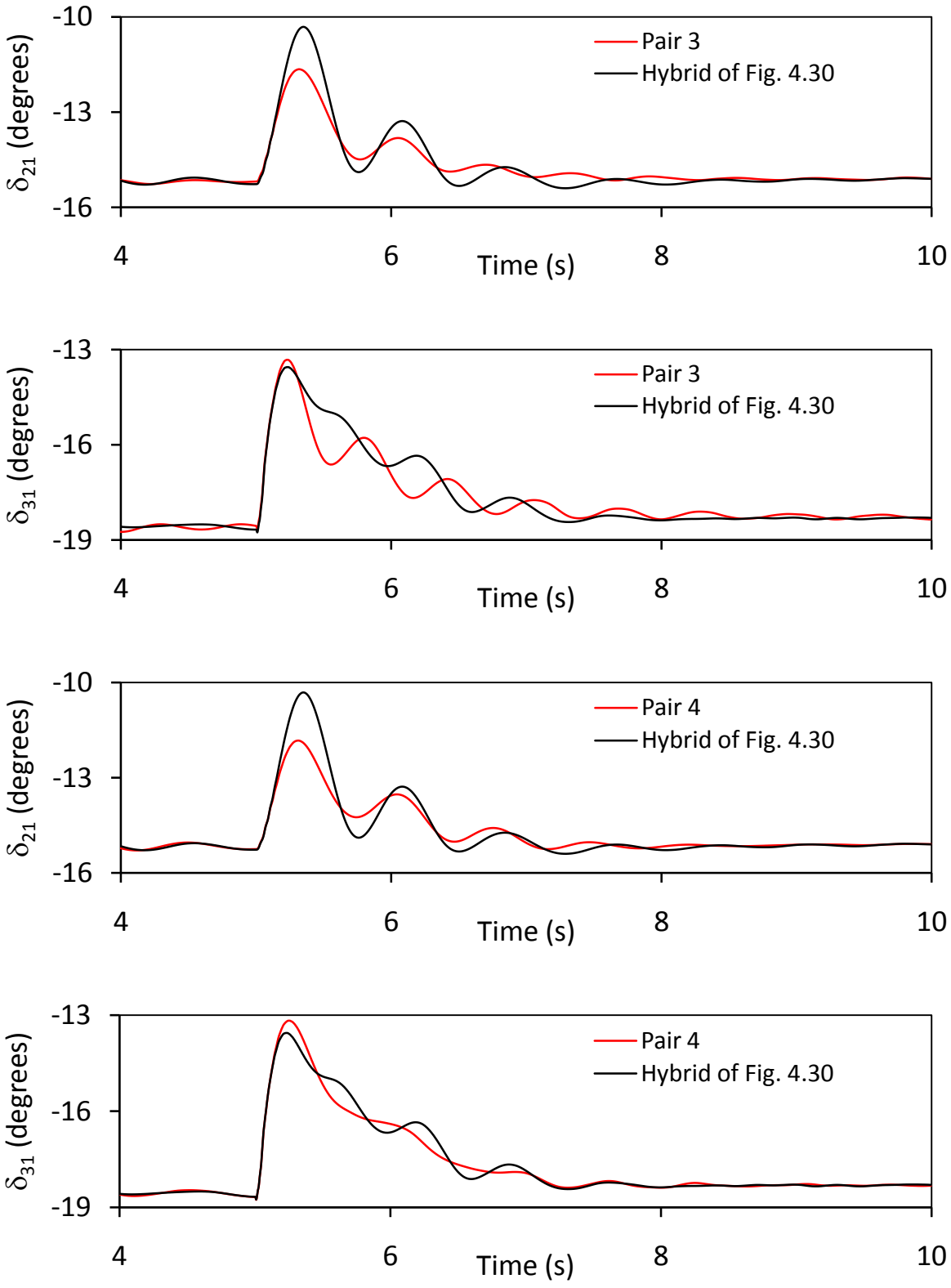


Figure 4.32: Continued.

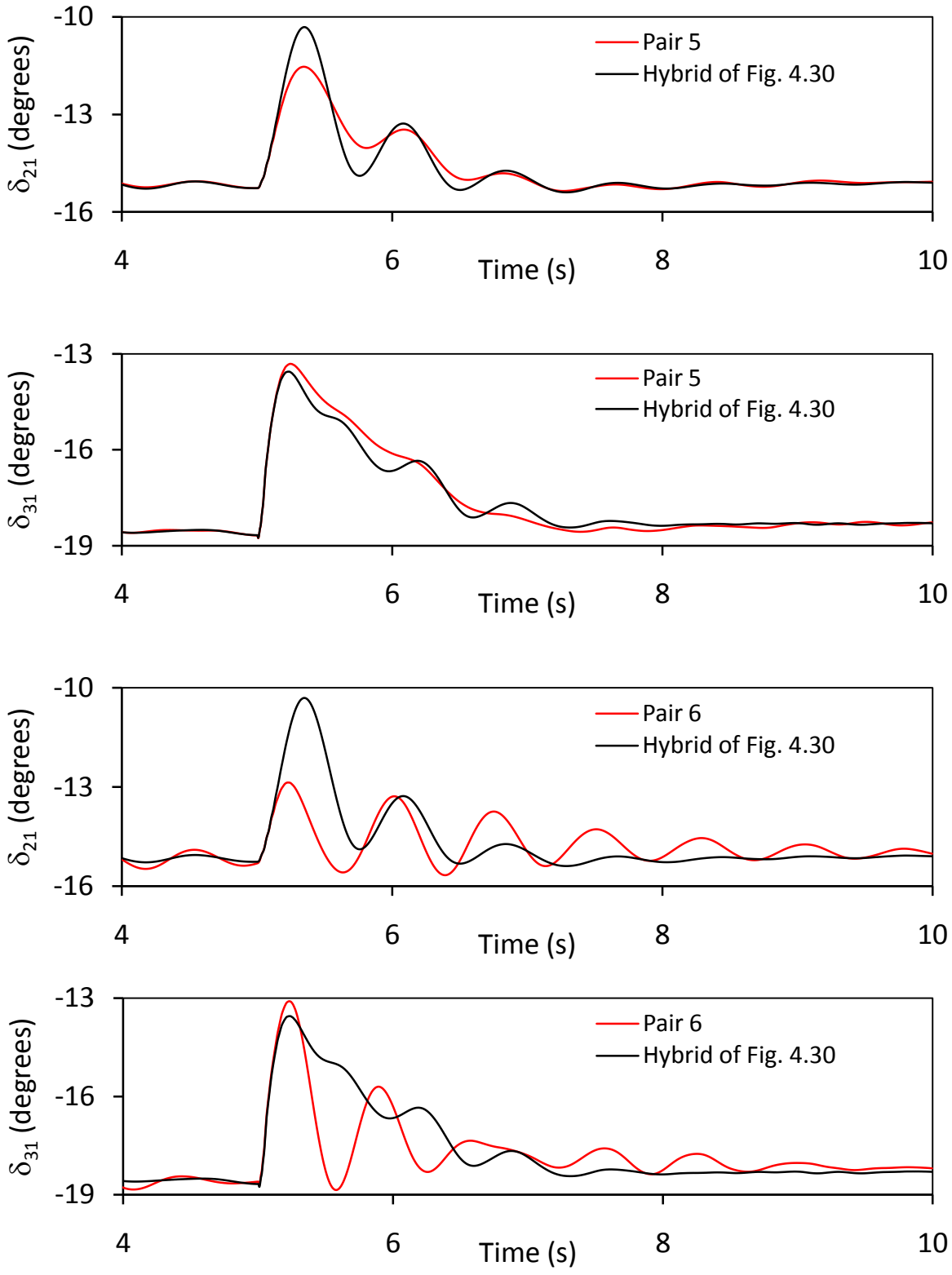


Figure 4.32: Continued.

Figure 4.33 illustrates the three-phase voltages, $V_{X\text{-}Y}$, across the hybrid single-phase SSSC compensation scheme (installed in L_1) of Figure 3.5 during and after clearing the three-phase fault of Figure 4.32 with pair 5. The system phase imbalance during the disturbance is clearly noticeable especially in phase C.

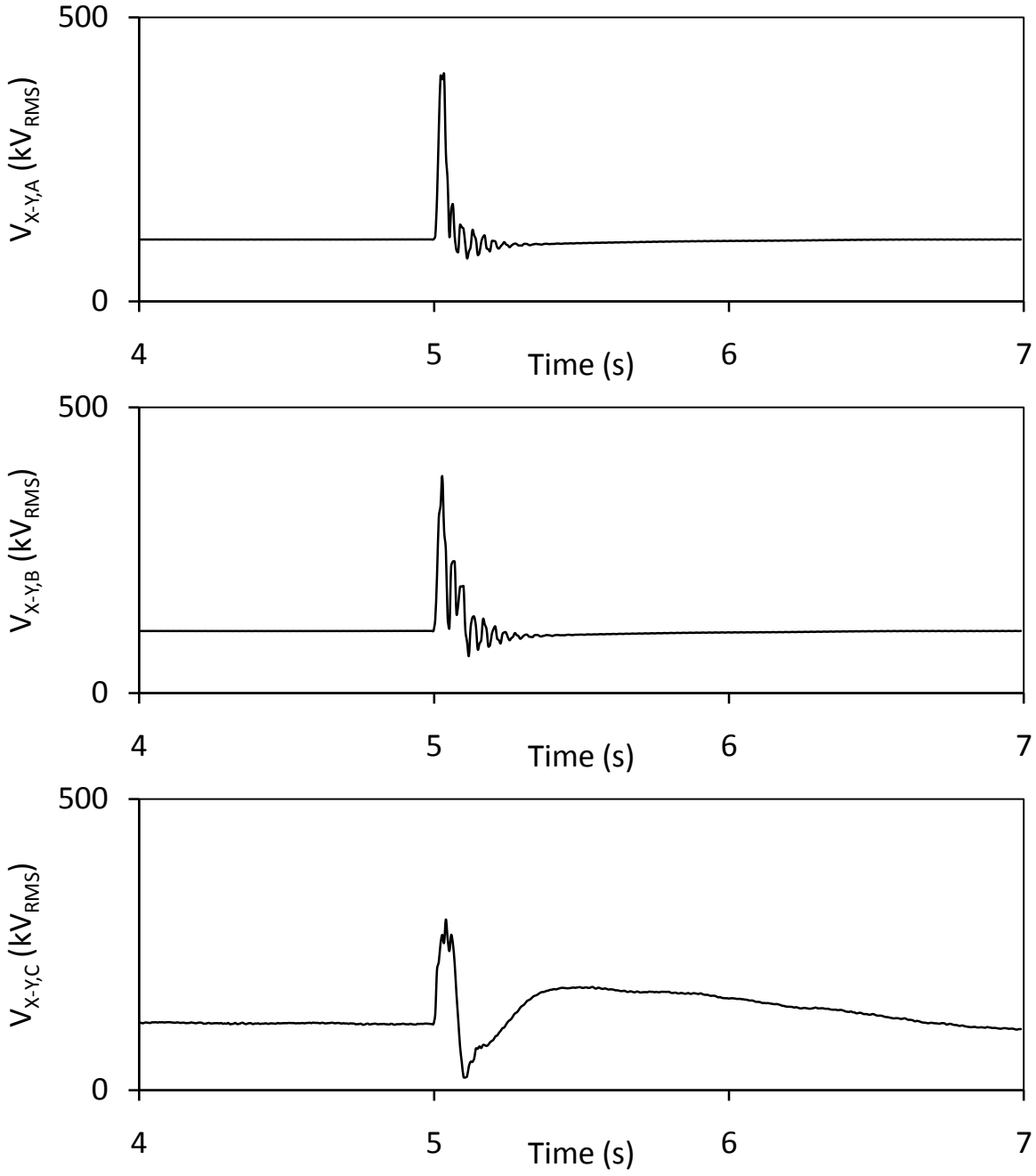


Figure 4.33: Phase voltages, $V_{X\text{-}Y}$ across the single-phase-SSSC of Fig. 3.5 during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study IV at a different loading profile, dual-channel supplemental controllers, pair 5, scheme in L_1).

4.7 Case Study V: The Hybrid Single-Phase-SSSC Compensation Scheme is Installed in Lines L_1 and L_3

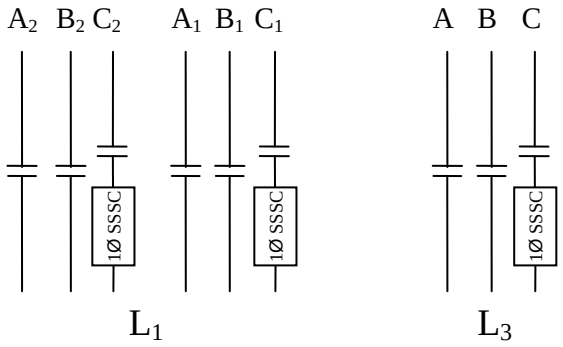


Figure 4.34: Case Study V: The hybrid single-phase-SSSC compensation scheme is installed in lines L_1 and L_3.

In this case study, the hybrid single-phase-SSSC compensation scheme is installed in the uncompensated line, L_3, for the purpose of system dynamic reinforcement. As it can be seen from Figure 2.6, line L_3 is the direct interconnection between G_1 and G_2. Controlling the real power flow of this line would have a direct impact on the oscillations between these two generators.

The system pre-fault load flow for this case is shown in Figure 4.35 where it is assumed that the degree of compensation of L_1 and L_3 is 50% and that each single-phase-SSSC provides 50% of the total capacitive compensation. The disturbance is a three-cycle, three-phase fault at bus 4. The final results of the time-domain simulation studies (controller tuning) are compared with Case Study III and are shown in Figure 4.36. This figure illustrates the generator load angles, measured with respect to generator 1 load angle, during and after fault clearing. The transfer functions of the SSSC supplemental controllers with the stabilizing signal δ_{21} are given in Table 4.6.

As the result of the series compensation of L_3, the phase angles between buses 1 and 2 as well as between buses 1 and 3 are reduced and the real power transmitted between buses 1 and 2 is increased (from 567 MW, Figure 2.6 to 724 MW, Figure 4.35). The reductions in these phase angles are directly reflected into reductions in the initial values of the relative generator load angles δ_{21} and δ_{31} as it is shown in Figure 4.36. The figure also shows that the hybrid single-phase-SSSC supplemental controllers provide very effective damping to system oscillations.

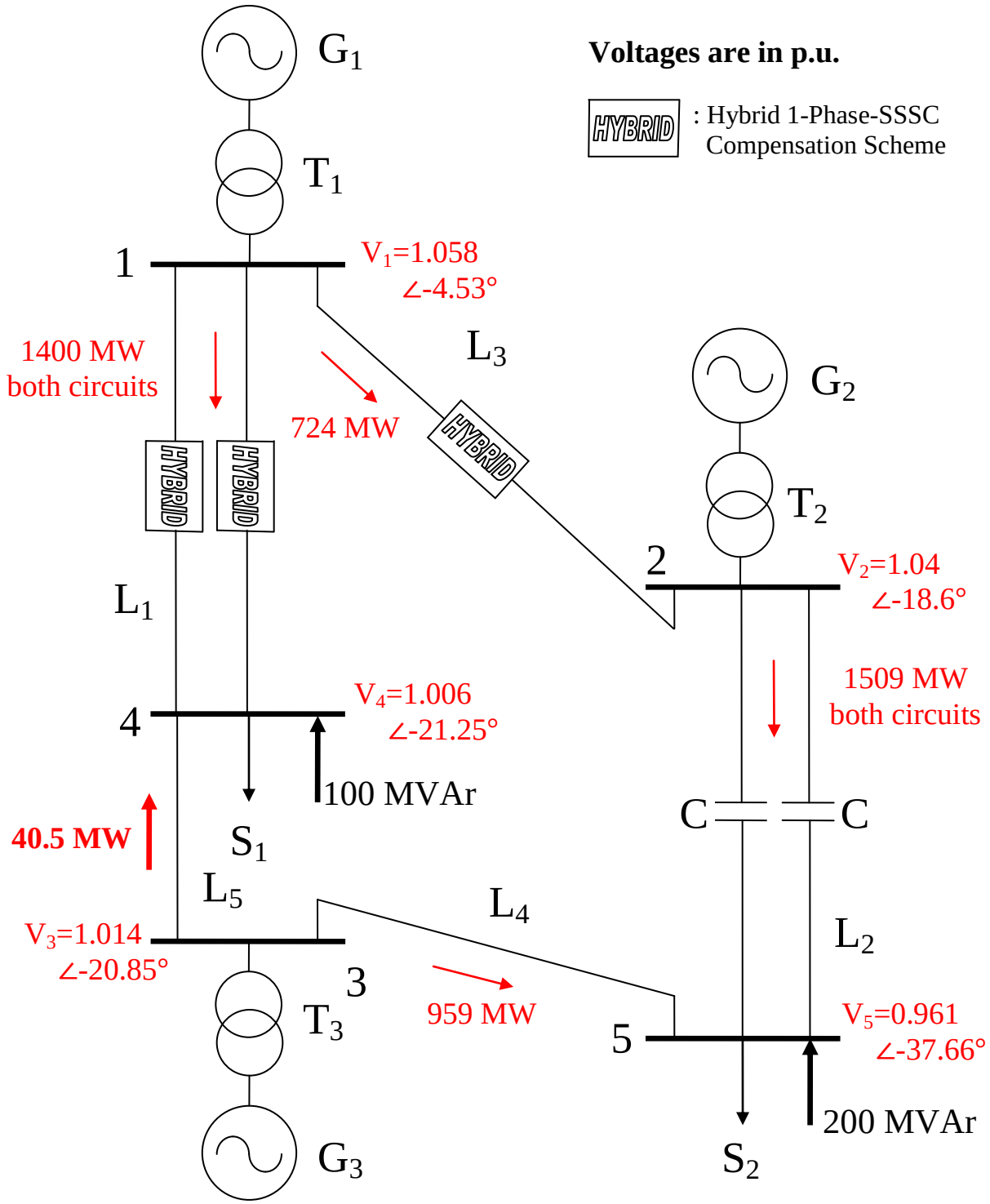


Figure 4.35: Power flow results of bus voltages and line real power flows of the system under study for Case Study V.

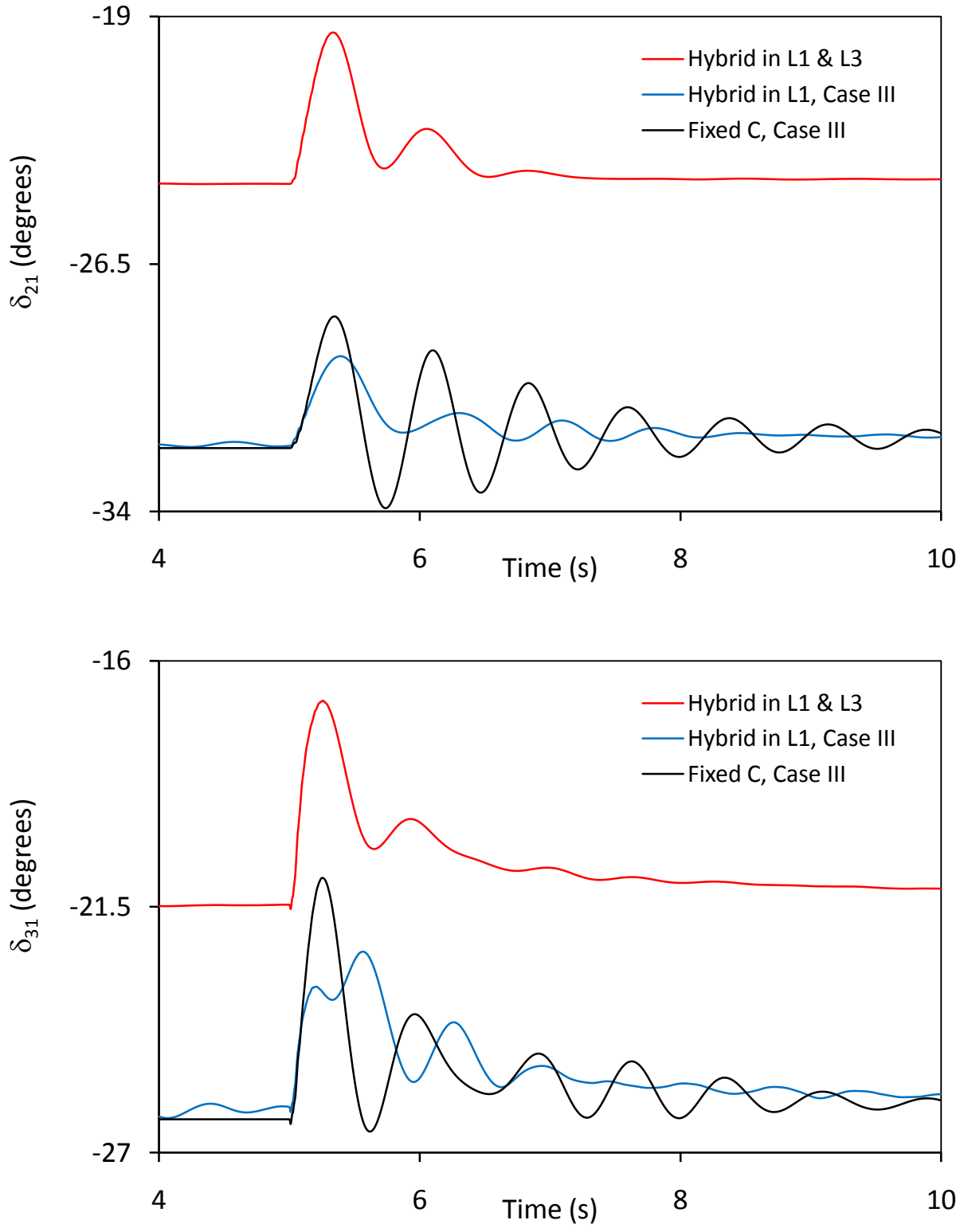


Figure 4.36: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 4 (Case Study V, stabilizing signals: δ_{21}).

Table 4.6: Transfer functions of the SSSC supplemental controllers with the stabilizing signal δ_{21} (Case V).

Each SSSC in L_1	SSSC in L_3
$G(s) = 0.025 \frac{15}{(s+15)} \frac{2s}{(2s+1)}$	$G(s) = 0.3 \frac{15}{(s+15)} \frac{2s}{(2s+1)}$

4.8 Summary

In this chapter, the effectiveness of the hybrid single-phase-SSSC compensation scheme in damping power system oscillations resulting from clearing system faults is investigated through several case studies of time-domain simulations. In this context, the effects of the number and locations of the schemes installed in the system, the SSSC supplemental controller structures and their stabilizing signals as well as the system load profiles on damping power system oscillations are explored. The main conclusions drawn from the results of these studies are presented in the next chapter.

Chapter 5

SUMMARY AND CONCLUSIONS

5.1 Summary

Oscillations of active power in power transmission systems may arise in corridors between generating areas as a result of poor damping of the interconnection, particularly during heavy power transfer. Such oscillations can be excited by a number of reasons such as line faults, switching of lines or a sudden change of generator output. The presence of active power oscillations acts to limit the power transmission capacity of interconnections between areas or transmission regions.

As a result of the FACTS initiative, considerable effort has been spent in the last two decades on the development of power electronic-based power flow controllers. The potential benefits of these FACTS controllers are now widely recognized by the power system engineering and the transmission and distribution communities. Although there is no stand-alone SSSC in service, it has a potential to be an attractive and very effective controller for power flow control and system oscillations damping. This thesis reports the results of the investigations that were carried out to explore the effectiveness of the hybrid single-phase-SSSC compensation scheme in damping power system oscillations in multi-machine power systems.

A brief review of the benefits of series compensation of transmission lines is presented in Chapter 1. The inability of series capacitors in providing adequate damping to power system oscillations as well as their contribution to the subsynchronous resonance phenomenon are also discussed in this chapter.

In Chapter 2, the system used in the studies conducted in this thesis is introduced and the mathematical models of its components are presented. The results of digital time-domain simulations of a case study for the system with only fixed capacitance compensation during a three-phase fault are also presented in this chapter.

In Chapter 3, the concept of series capacitive compensation, synchronous voltage source and the hybrid series capacitive compensation scheme are presented. The single-phase

converter, SPWM technique as well as the single-phase three-level SSSC and its modeling in the EMTP-RV are also presented.

In Chapter 4, several case studies investigating the effects of the location of the hybrid single-phase-SSSC compensation scheme, the degree of compensation provided by the scheme, the SSSC supplemental controller structure, the stabilizing signal as well as the loading profile on the damping of power system oscillations are documented. These studies are intended to demonstrate the effectiveness of the proposed scheme in damping power system oscillations resulting from clearing system faults.

5.2 Conclusions

The studies conducted in this thesis yield the following conclusions for the system under study:

1. The series capacitor compensated system is first swing stable for three-phase faults, but the post-contingency oscillations are not well damped.

2. Although the system has two natural modes of oscillation, generators 2 and 3 tend to oscillate at a single frequency (approximately 1.4 Hz).

3. The hybrid single-phase-SSSC compensation scheme has shown to be, in general, very effective in damping power system oscillations at different loading profiles.

4. Increasing the proportion of the single-phase-SSSC to the fixed capacitor of its phase results in improving the damping of system oscillations. Increasing the proportion of the hybrid single-phase-SSSC compensation scheme to the total fixed capacitor compensation (i.e. installing the scheme in more transmission line circuits replacing fixed capacitor compensation) enhances significantly the damping of system oscillations. Choosing the values of such two proportion options can be considered as an optimization task between dynamic stability improvements and economical and reliability advantages of fixed series capacitors.

5. The performance of the SSSC supplemental controller when the deviation of generator 2 load angle, with respect to generator 1 load angle, is used as the stabilizing signal is better

than when the deviations in the generator speeds or the transmission line real power flows are utilized.

6. In the majority of the case studies, adequate power system oscillation damping is obtained with proportional-type SSSC supplemental controllers.

7. With the hybrid single-phase-SSSC compensation scheme installed in all circuits of lines L_1 and L_2, the best performance of the SSSC supplemental controllers is obtained when the deviation of generator 3 load angle, with respect to generator 1 load angle, is used as the stabilizing signal for all controllers.

8. A dual-channel SSSC supplemental controller is more effective in damping power system oscillations than a single-channel controller. In this regard, the best two signals are found out to be the deviation of generator 3 load angle, with respect to generator 1 load angle and the real power flow in line L_2.

9. Overall, the best damping of the relative load angle responses are achieved when the hybrid single-phase-SSSC is installed in line L_3 as well as in the two circuits of line L_1.

10. The reduction of the generator first swings depends on the proportion of the hybrid single-phase-SSSC compensation scheme to the total fixed capacitor compensation in the system. It is observed, however, that in one case there is a slight increase in the first swing of one generator. It should be emphasized here that the main task of the supplemental controller of the hybrid single-phase-SSSC compensation scheme is to damp power system oscillations in the "already stable" system under study. For transient stability control of marginally stable power systems, different SSSC control methodologies are usually used.

As is the case with all research, many venues were not fully explored and many new questions came to light as a result of this research project. It is believed, however, that some key questions regarding the use of the hybrid single-phase-SSSC compensation scheme in damping power system oscillations in multi-machine power systems have been answered. It is hoped that this thesis will be of value to anyone working to improve the damping performance of the scheme in other similar systems.

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APPENDIX A

A.1 DATA OF THE SYSTEM UNDER STUDY

Synchronous Generators

Table A.1: Synchronous generator data.

	G_1	G_2	G_3
Rating, MVA	2400	1000	1100
Rated voltage, kV	26	26	26
Armature resistance, r_a, p.u.	0	0.0045	0.0045
Leakage reactance, x_l, p.u.	0.13	0.14	0.12
Direct-axis synchronous reactance, x_d, p.u.	1.79	1.65	1.54
Quadrature-axis synchronous reactance, x_q, p.u.	1.71	1.59	1.5
Direct-axis transient reactance, $x_d^{'}$, p.u.	0.169	0.25	0.23
Quadrature-axis transient reactance, $x_q^{'}$, p.u.	0.228	0.46	0.42
Direct-axis subtransient reactance, $x_d^{''}$, p.u.	0.135	0.2	0.18
Quadrature-axis subtransient reactance, $x_q^{''}$, p.u.	0.2	0.2	0.18
Direct-axis transient open-circuit time constant, $T_{do}^{'}$, s	4.3	4.5	3.7
Quadrature-axis transient open-circuit time constant, $T_{qo}^{'}$, s	0.85	0.55	0.43
Direct-axis subtransient open-circuit time constant, $T_{do}^{''}$, s	0.032	0.04	0.04
Quadrature-axis subtransient open-circuit time constant, $T_{qo}^{''}$, s	0.05	0.09	0.06
Zero-sequence reactance, x_o, p.u.	0.13	0.14	0.12
Inertia constant, H, s	7	3.7	3.12

Transformers

Table A.2: Transformer data.

	T_1	T_2	T_3
Rating, MVA	2400	1000	1100
Rated voltage, kV	26/500	26/500	26/500
Resistance, r_T , p.u.	0	0	0
Leakage reactance, x_T , p.u.	0.1	0.1	0.1

Transmission Lines

All transmission lines have the same series impedance and shunt admittance per unit length.

$$Z_{T.L.series} = 0.01864 + j\,0.3728\ \Omega / km$$

$$Y_{T.L.shunt} = j\,4.4739\ \mu S / km$$

Transmission voltage = 500 kV

System Loads

$$S_1 = 1400 + j\,200\ MVA$$

$$S_2 = 2400 + j\,300\ MVA$$

Excitation System

Table A.3: Excitation system data.

K_A = 2	T_A = 0.04 s
K_E = 1.0	T_E = 0.01s
K_F = 0.03	T_F = 1.0 s
Lim_max = 4.75 p.u.	*Lim_min* = -4.75 p.u.

A.2 DATA OF THE CONTROLLERS FOR CASE STUDIES

Table A.4: Data for SSSCs on L_1 and L_2.

Case	Controller							
	Line 1				Line 2			
	Injected Voltage Magnitude Control		DC Voltage Control		Injected Voltage Magnitude Control		DC Voltage Control	
	K_p	K_i	K_p	K_i	K_p	K_i	K_p	K_i
Case I	0.05	1.0	0.075	1.0	-	-	-	-
Case II	-	-	-	-	0.05	2.0	0.1	2.0
Case III	0.05	1.0	0.075	1.0	-	-	-	-
Case IV	0.05	1.0	0.075	1.0	0.05	2.0	0.1	2.0
Case IV – Different Loading	0.05	1.0	0.075	0.5	0.05	2.0	0.1	2.0
Case in Appendix C	-	-	-	-	0.05	2.0	0.1	2.0

DC Capacitors: $C_1 = C_2 = 10$ mF, ($V_{dc} = 18$ kV)

Table A.5: Data for SSSCs on L_1 and L_3.

Case	Controller							
	Line 1				Line 3			
	Injected Voltage Magnitude Control		DC Voltage Control		Injected Voltage Magnitude Control		DC Voltage Control	
	K_p	K_i	K_p	K_i	K_p	K_i	K_p	K_i
Case V	0.5	3.0	0.2	0.7	1.0	5.0	0.1	1.0

DC Capacitors: $C_1 = C_2 = 10$ mF, ($V_{dc} = 18$ kV)

APPENDIX B

ADDITIONAL CASE STUDY:

THE HYBRID SINGLE-PHASE-SSSC COMPENSATION SCHEME IS INSTALLED IN BOTH CIRCUITS OF LINE L_2

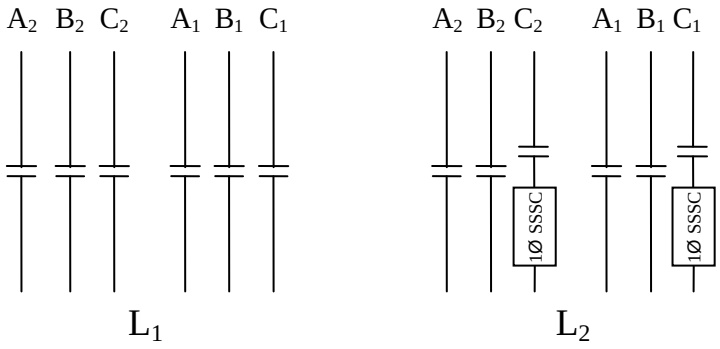

Figure B.1: The hybrid single-phase-SSSC compensation scheme is installed in both circuits of Line L_2.

Each SSSC provides 50% of the total capacitive compensation and the stabilizing signal is δ_{21} for both controllers. The generator load angles and speeds, measured with respect to generator 1 load angle and speed, and the transmission line real power flow responses during and after clearing a three-cycle, three-phase fault at bus 5 are illustrated in Figures B.2 to B.4 for the case when the SSSC supplemental controllers are of a proportional type with a transfer function:

$$G_P(s) = -0.12\frac{15}{(s+15)}\frac{2s}{(2s+1)} \tag{B.1}$$

The comparison between Figures B.2 and 4.12 as well as between Figures B.3 and 4.13 shows that, installing the hybrid single-phase-SSSC compensation scheme in the second circuit of L_2 improves the system damping near steady-state, especially for δ_{21} and ω_{21}. The comparison also shows insignificant change in the damping of the system oscillations during the first cycle.

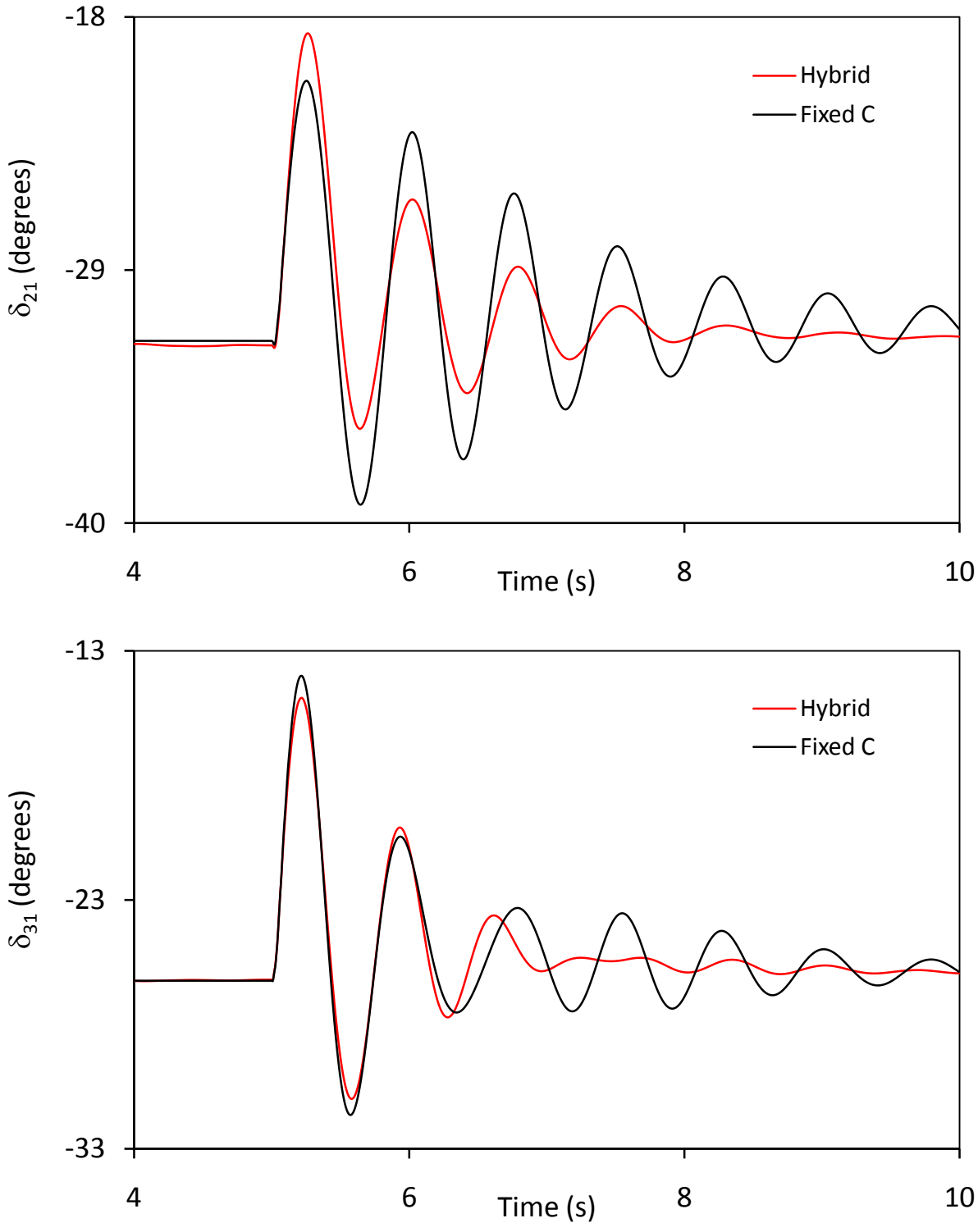

Figure B.2: Generator load angles, measured with respect to generator 1 load angle, during and after clearing a three-cycle, three-phase fault at bus 5 (stabilizing signal: δ_{21}).

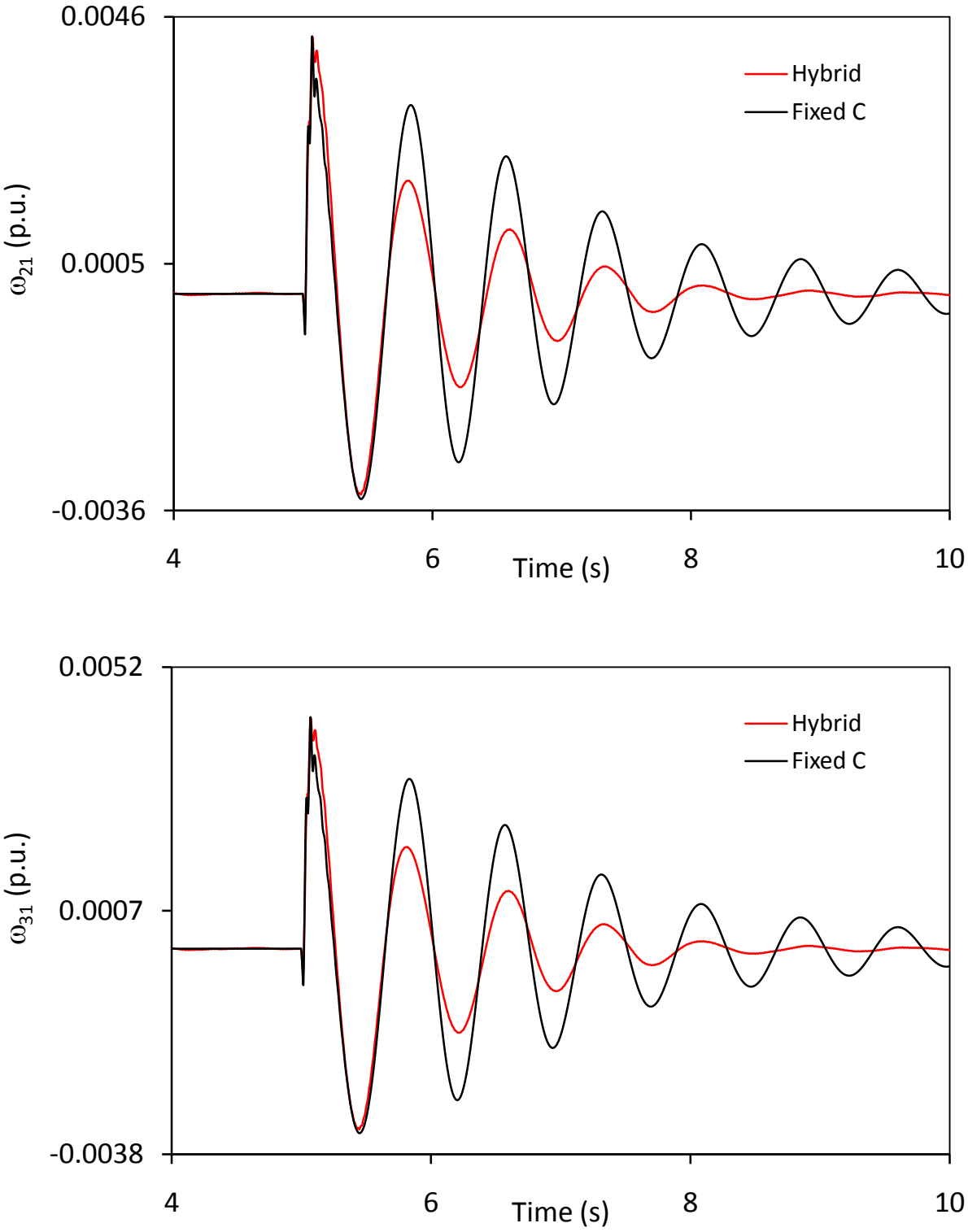

Figure B.3: Generator speeds, measured with respect to generator 1 speed, during and after clearing a three-cycle, three-phase fault at bus 5 (stabilizing signal: δ_{21}).

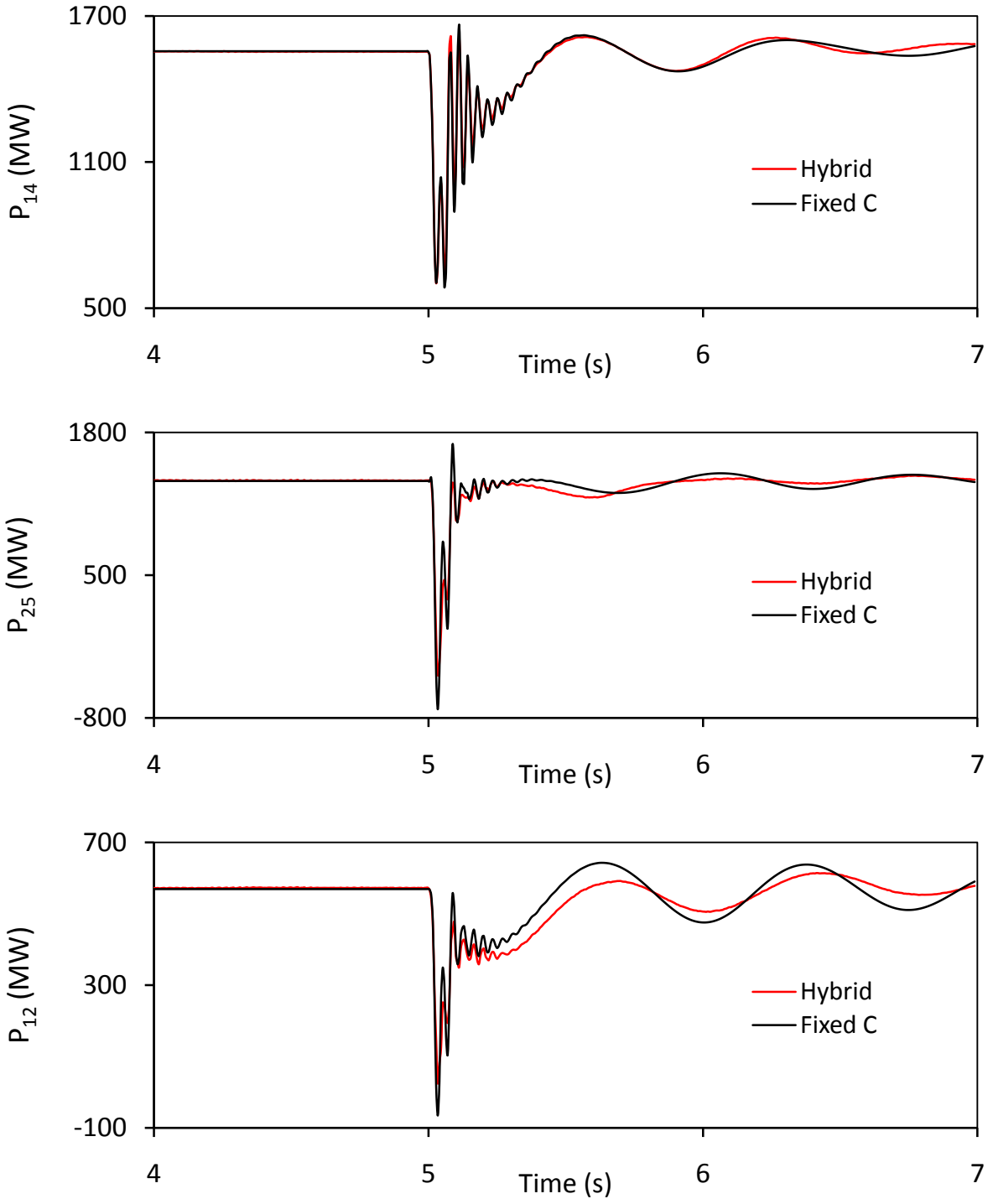

Figure B.4: Transmission line real power flows during and after clearing a three-cycle, three-phase fault at bus 5 (stabilizing signal: δ_{21}).

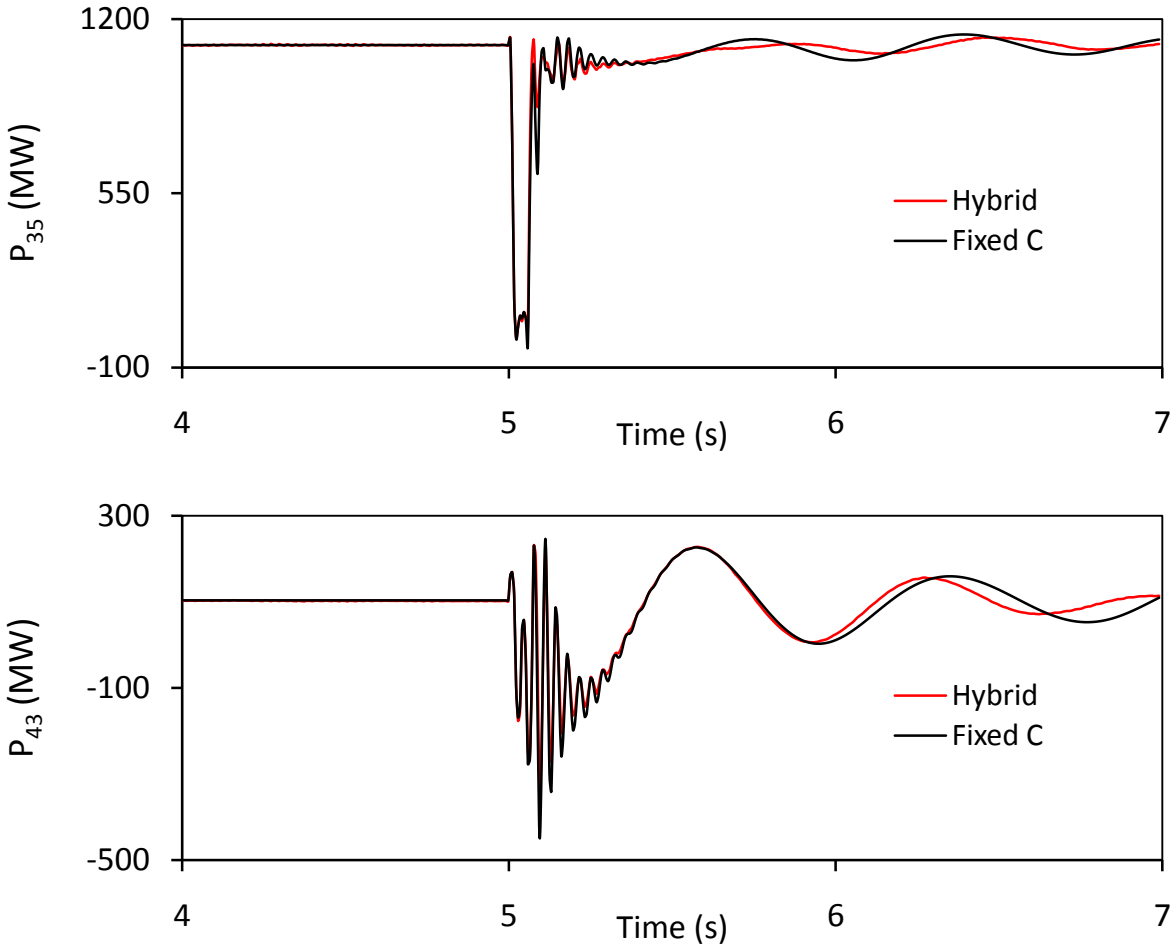

Figure B.4: Continued.